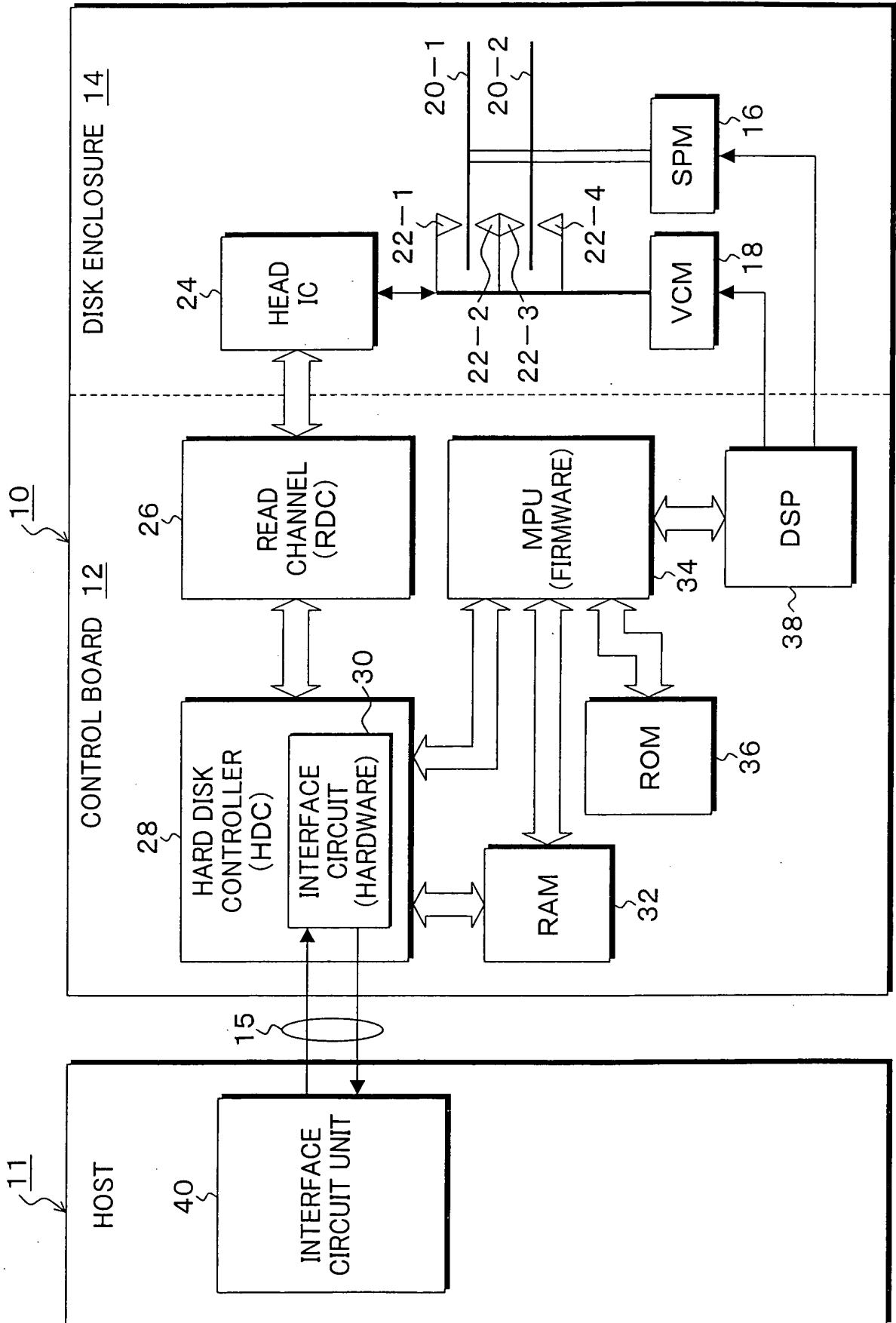


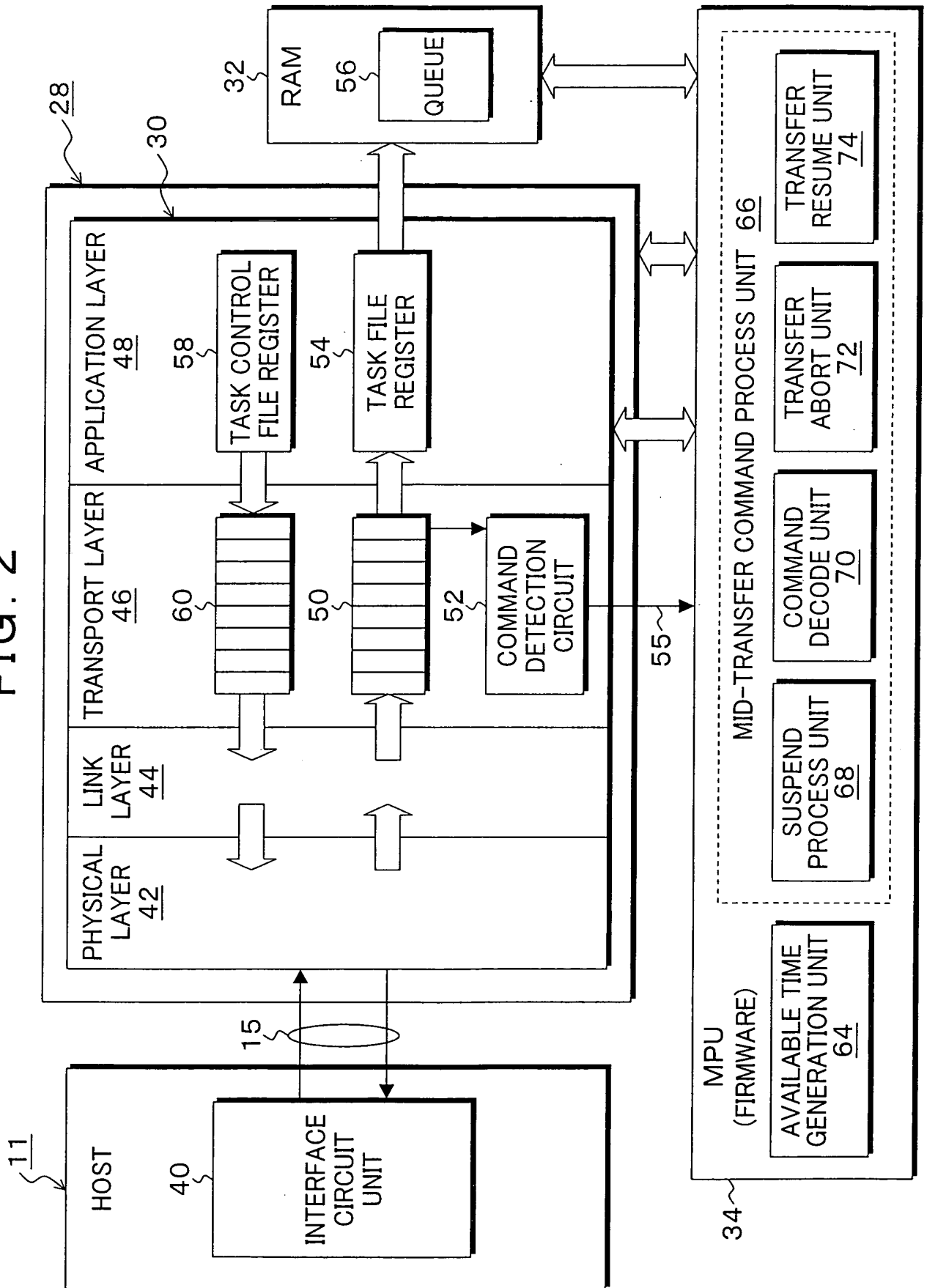
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FIG. 1



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FIG. 2



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FIG. 3A

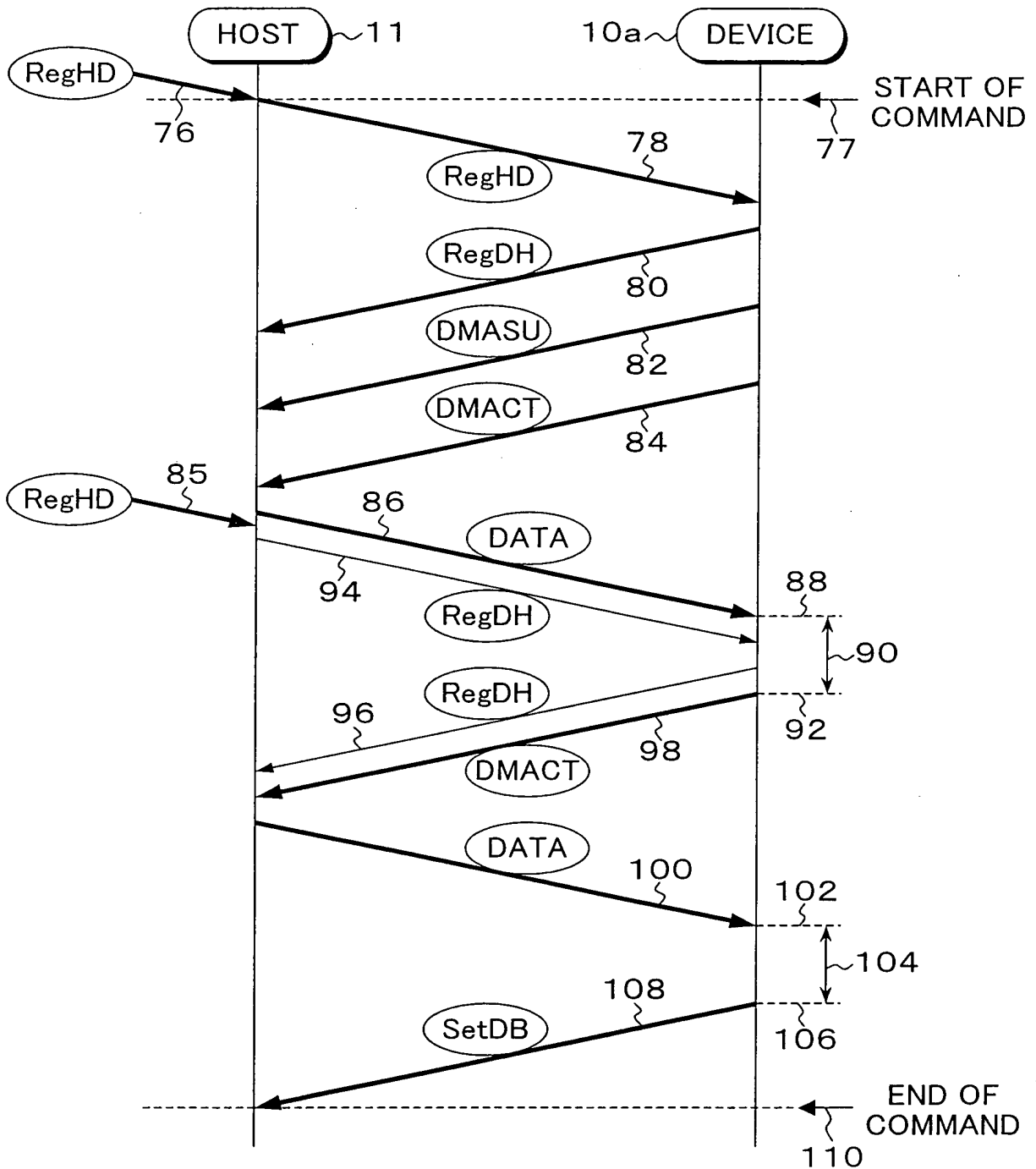
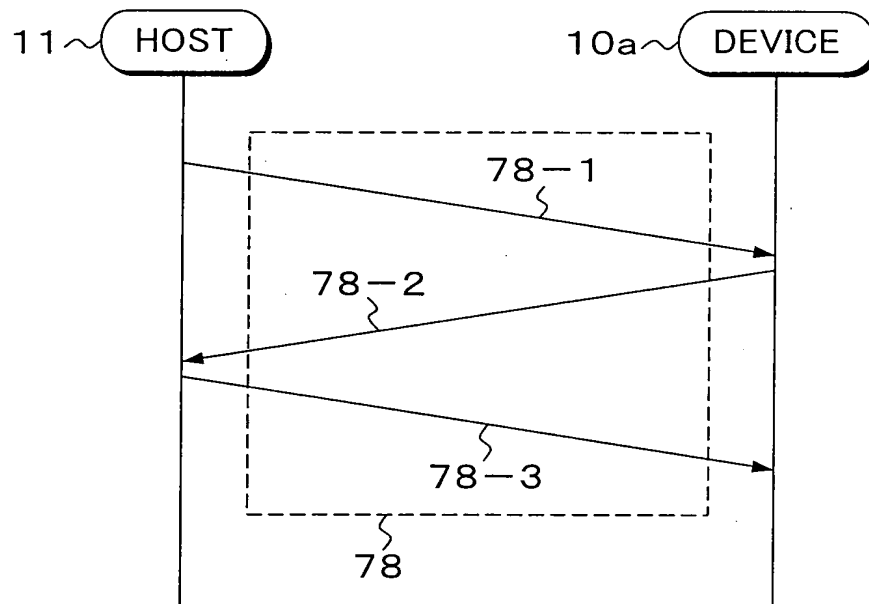
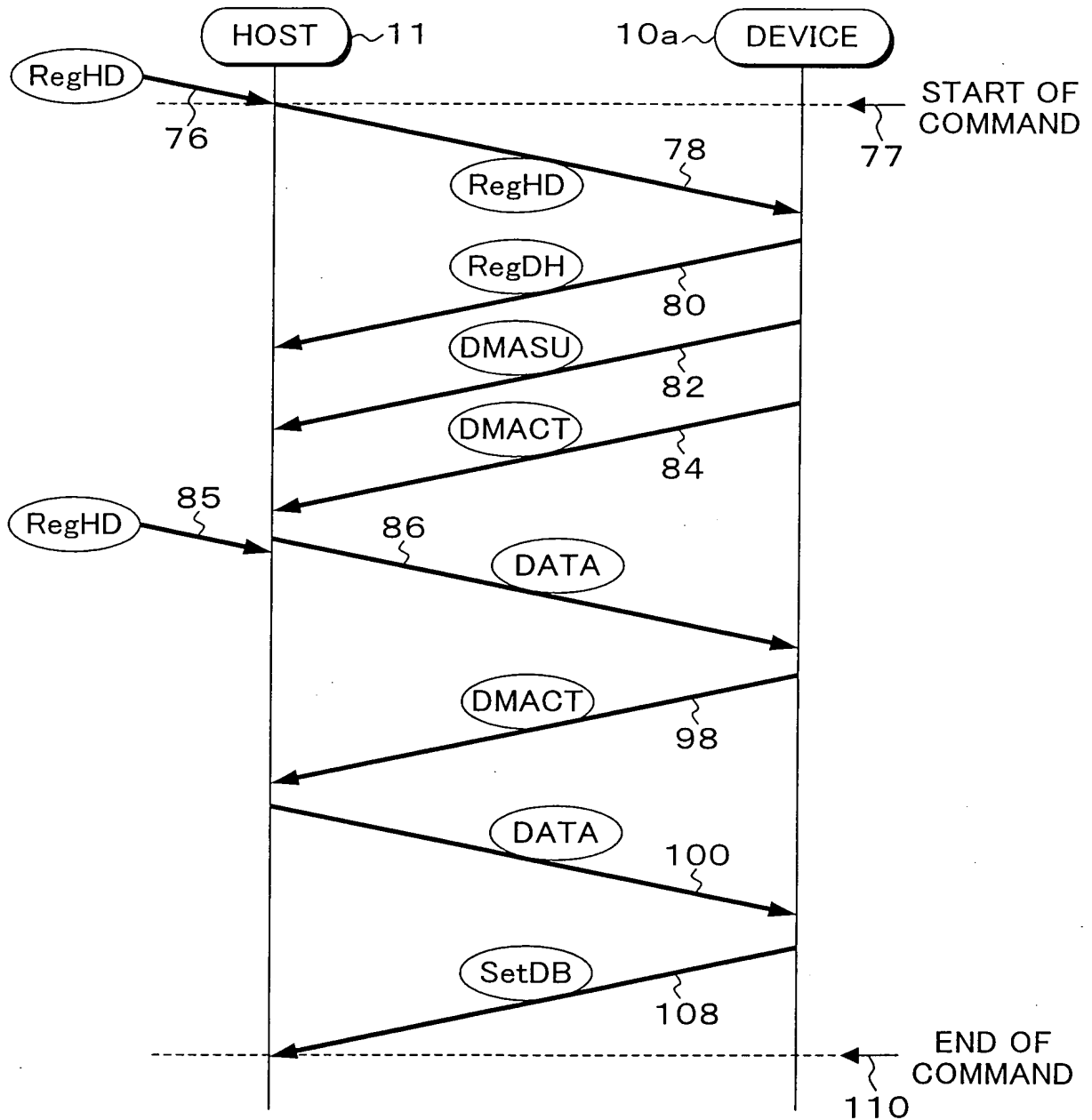


FIG. 3B



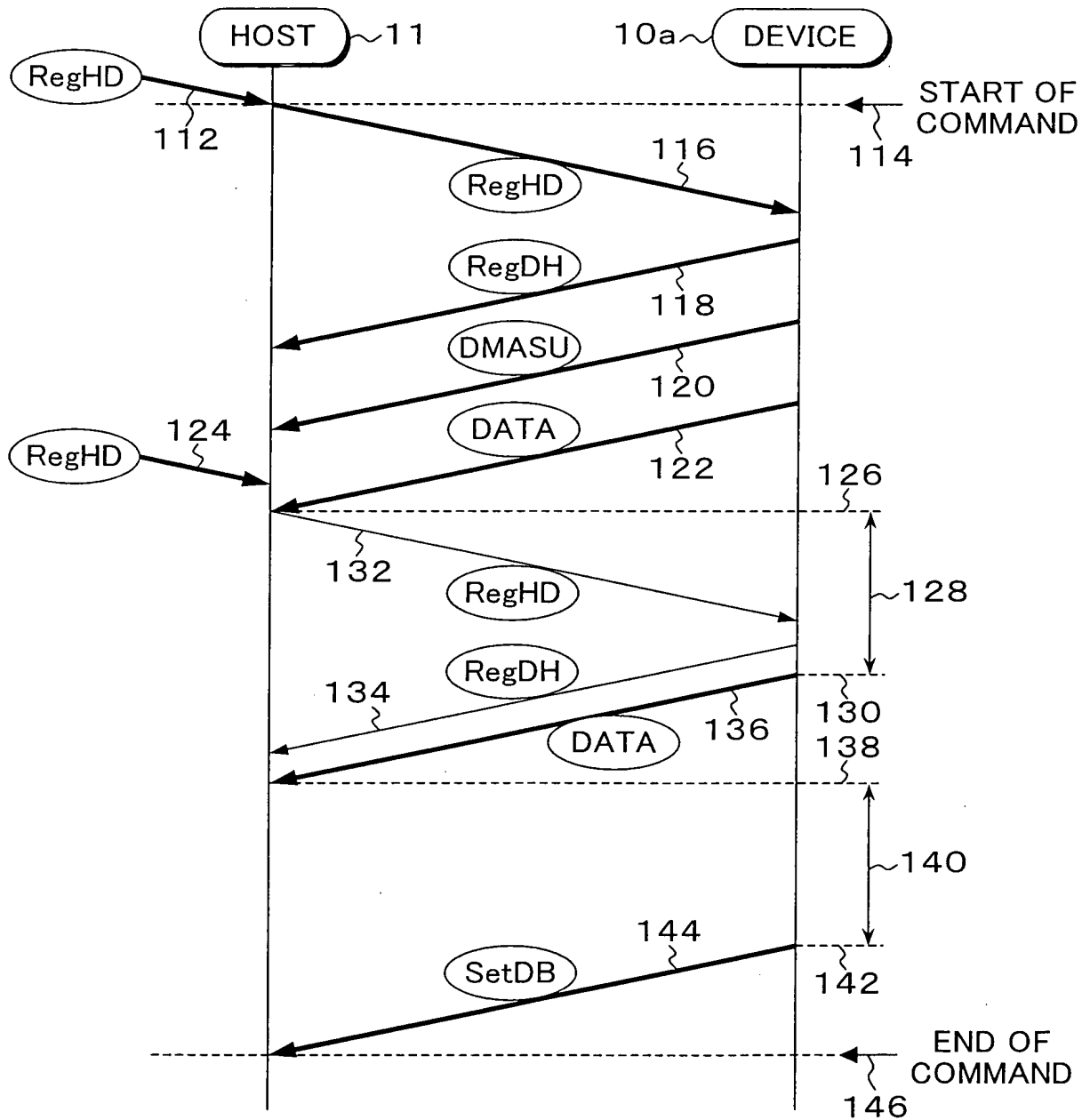
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FIG. 4



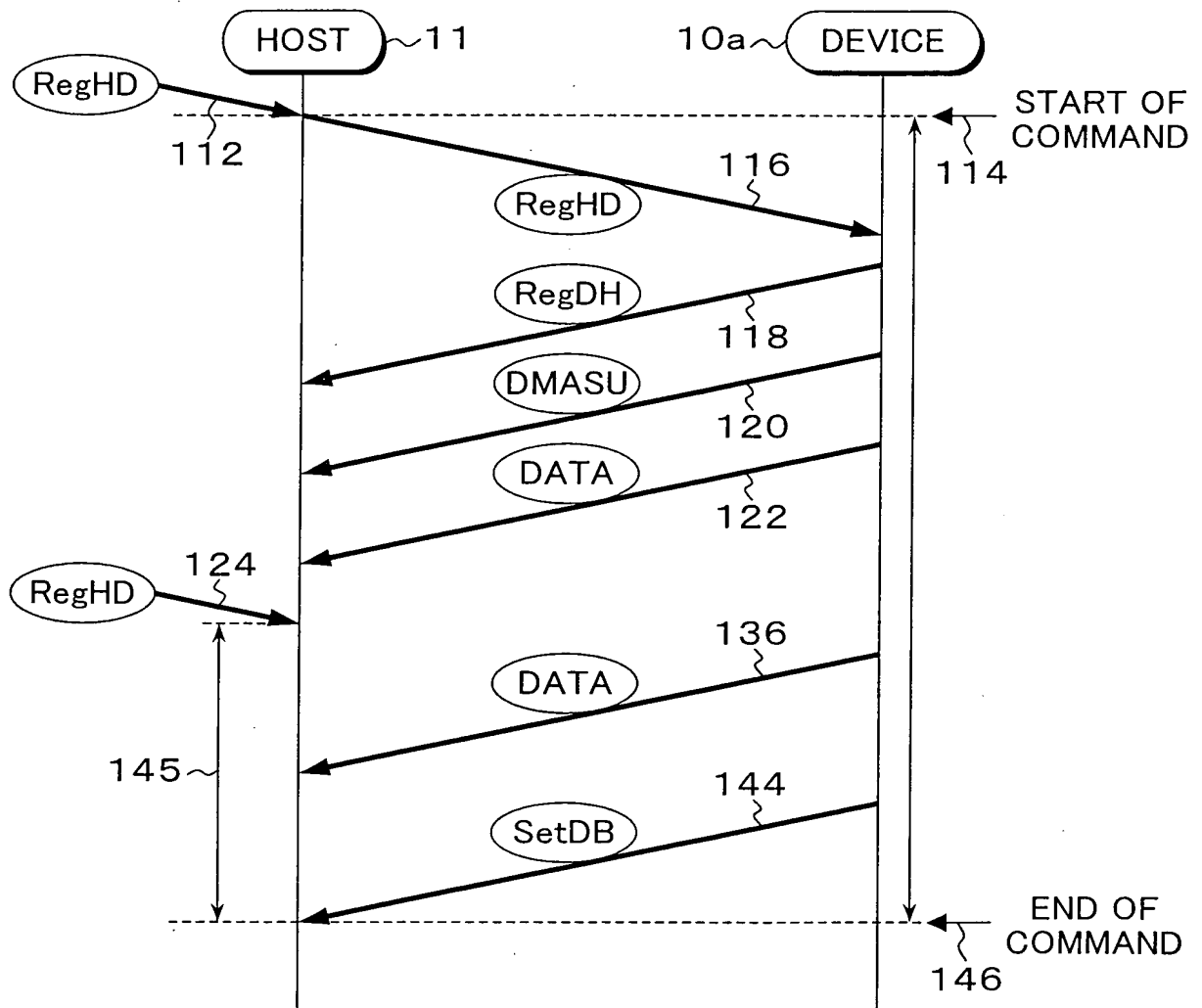
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FIG. 5



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PRIOR ART FIG. 6



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FIG. 7

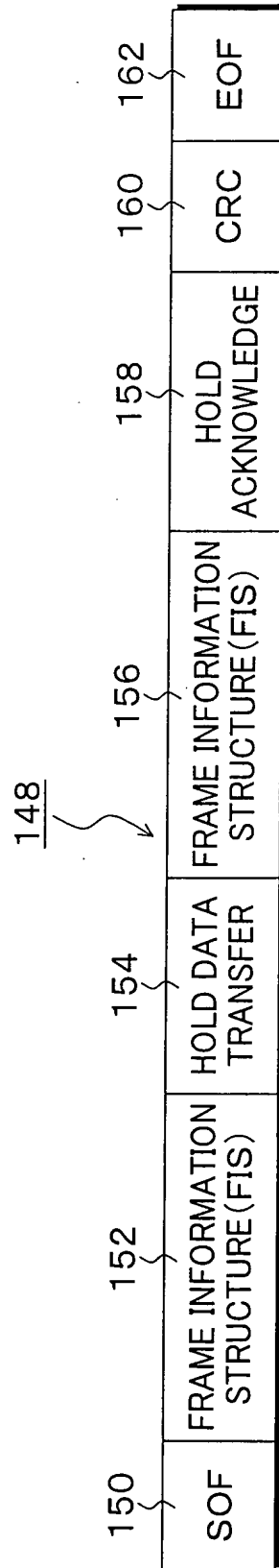


FIG. 8

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0	Features	Command	C	R	R	Reserved(0)	FIS Type(27h)
1	Dev/Head	Cyl High	Cyl Low				Sector Number
2	Features(exp)	Cyl High(exp)	Cyl Low(exp)				Sector Num(exp)
3	Control	Reserved(0)	Sector Count(exp)				Sector Count
4	Reserved(0)	Reserved(0)	Reserved(0)				Reserved(0)

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FIG. 9

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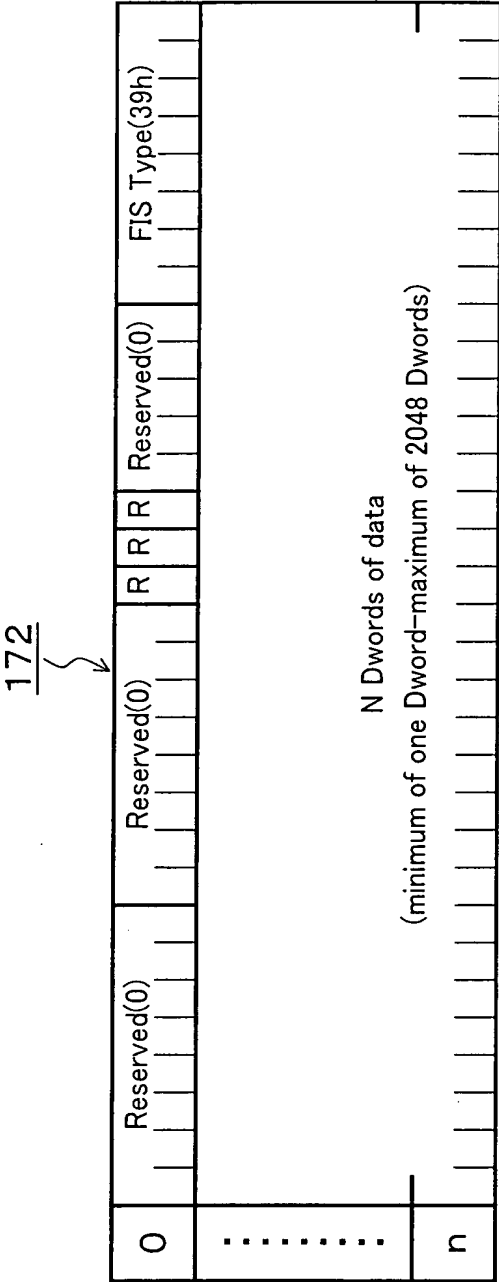
0	Error	Status	R	I	R	Reserved(0)	FIS Type(34h)
1	Dev/Head	Cyl High	Cyl Low				Sector Number
2	Reserved(0)	Cyl High(exp)	Cyl Low(exp)				Sector Num(exp)(0)
3	Reserved(0)	Reserved(0)	Sector Count(exp)				Sector Count
4	Reserved(0)	Reserved(0)	Reserved(0)				Reserved(0)

FIG. 11

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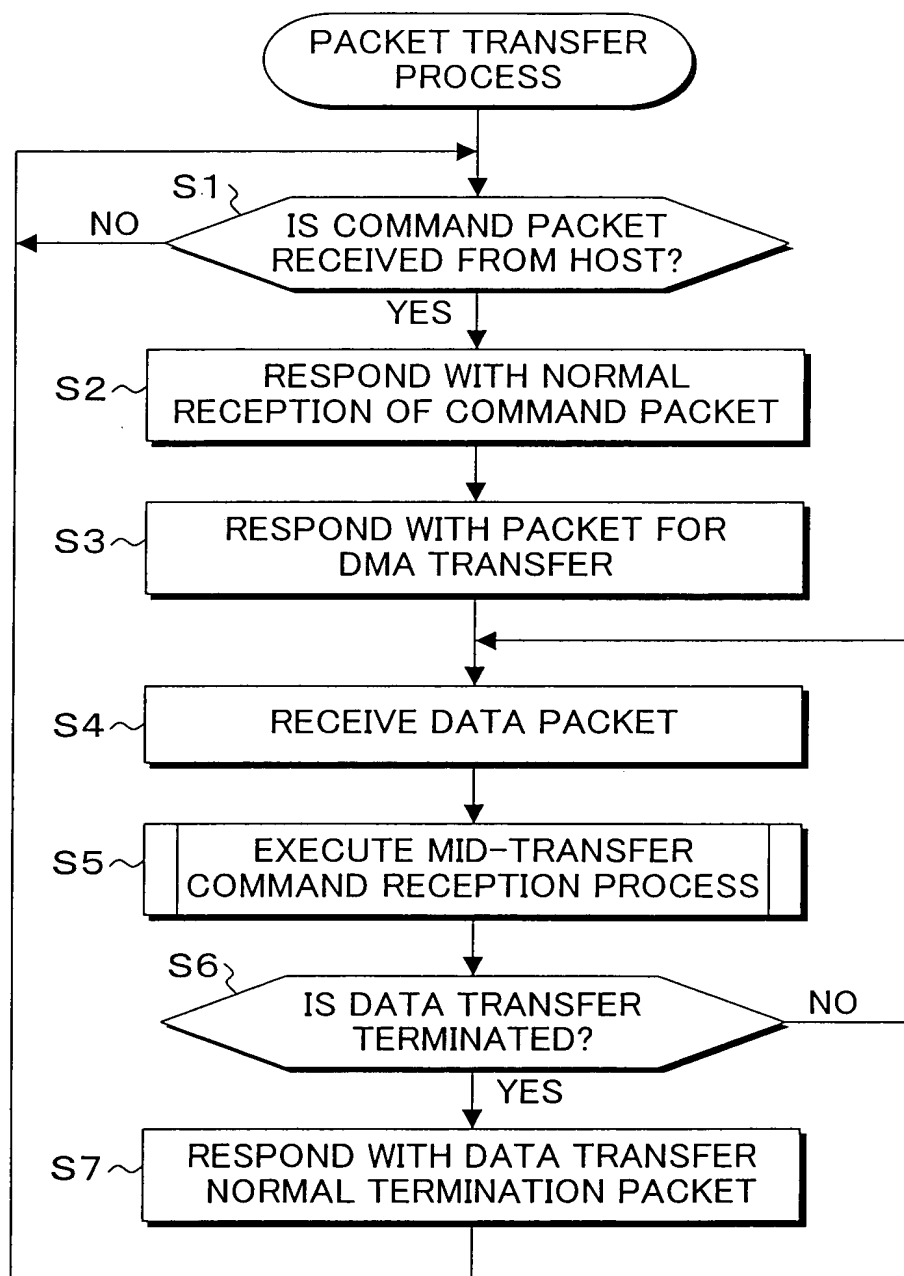


FIG. 12



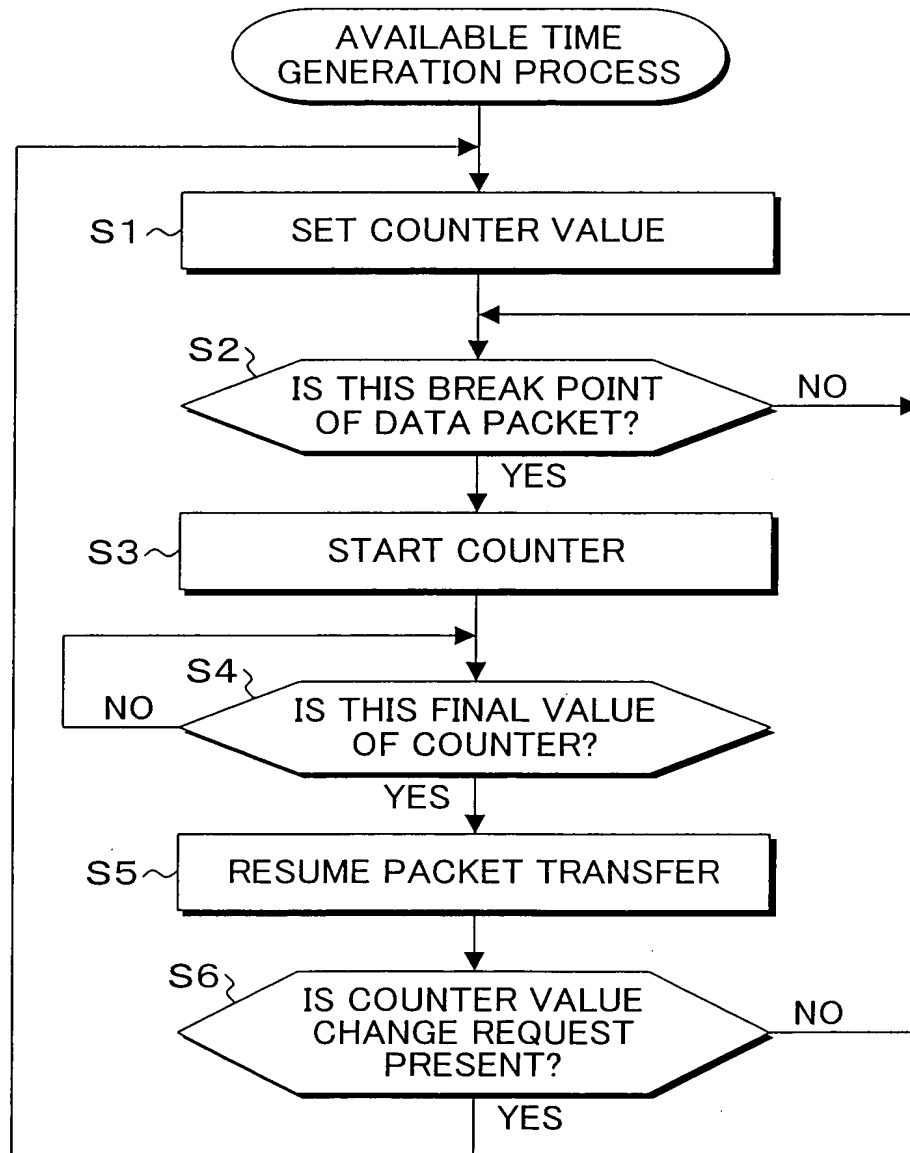
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FIG. 14



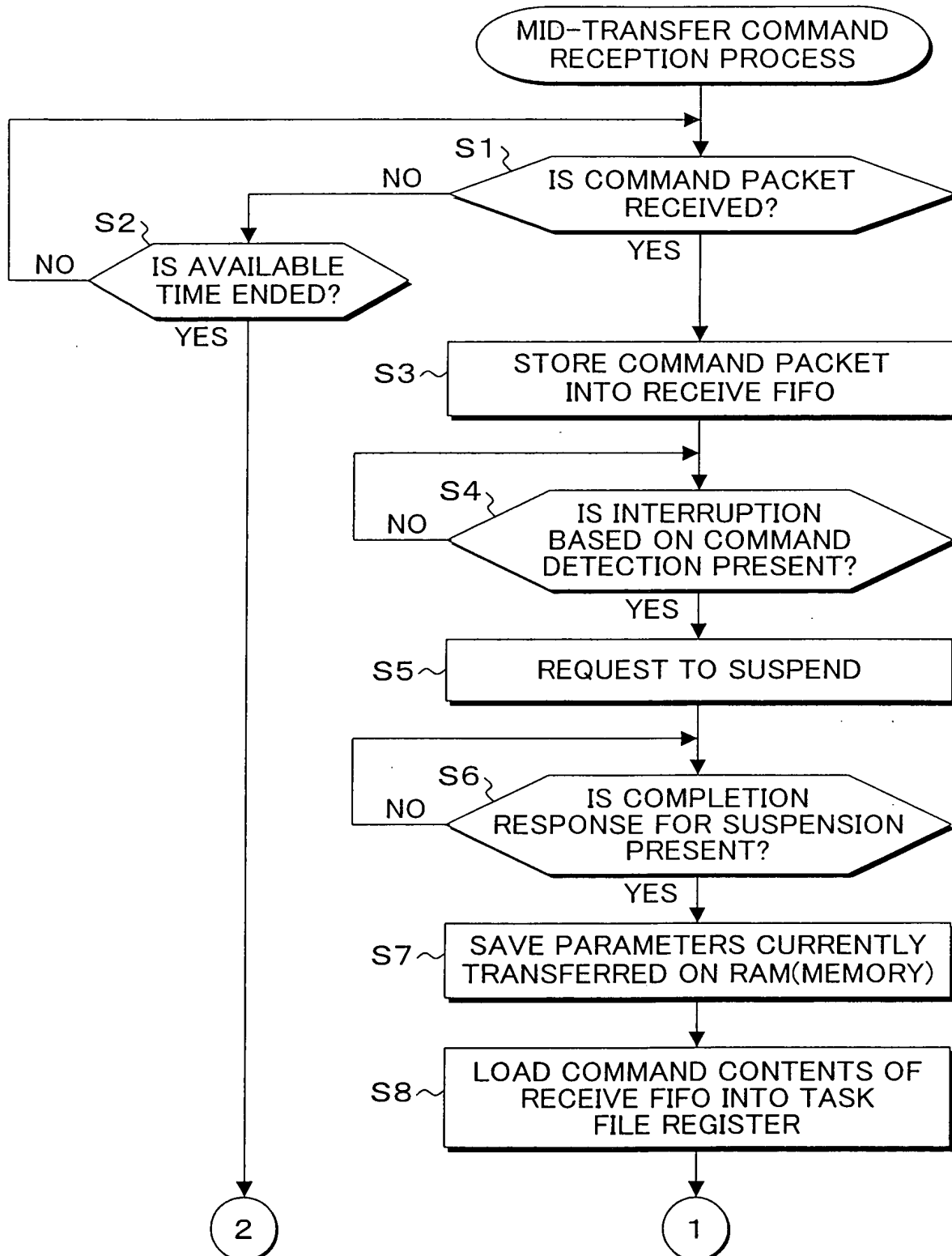
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FIG. 15



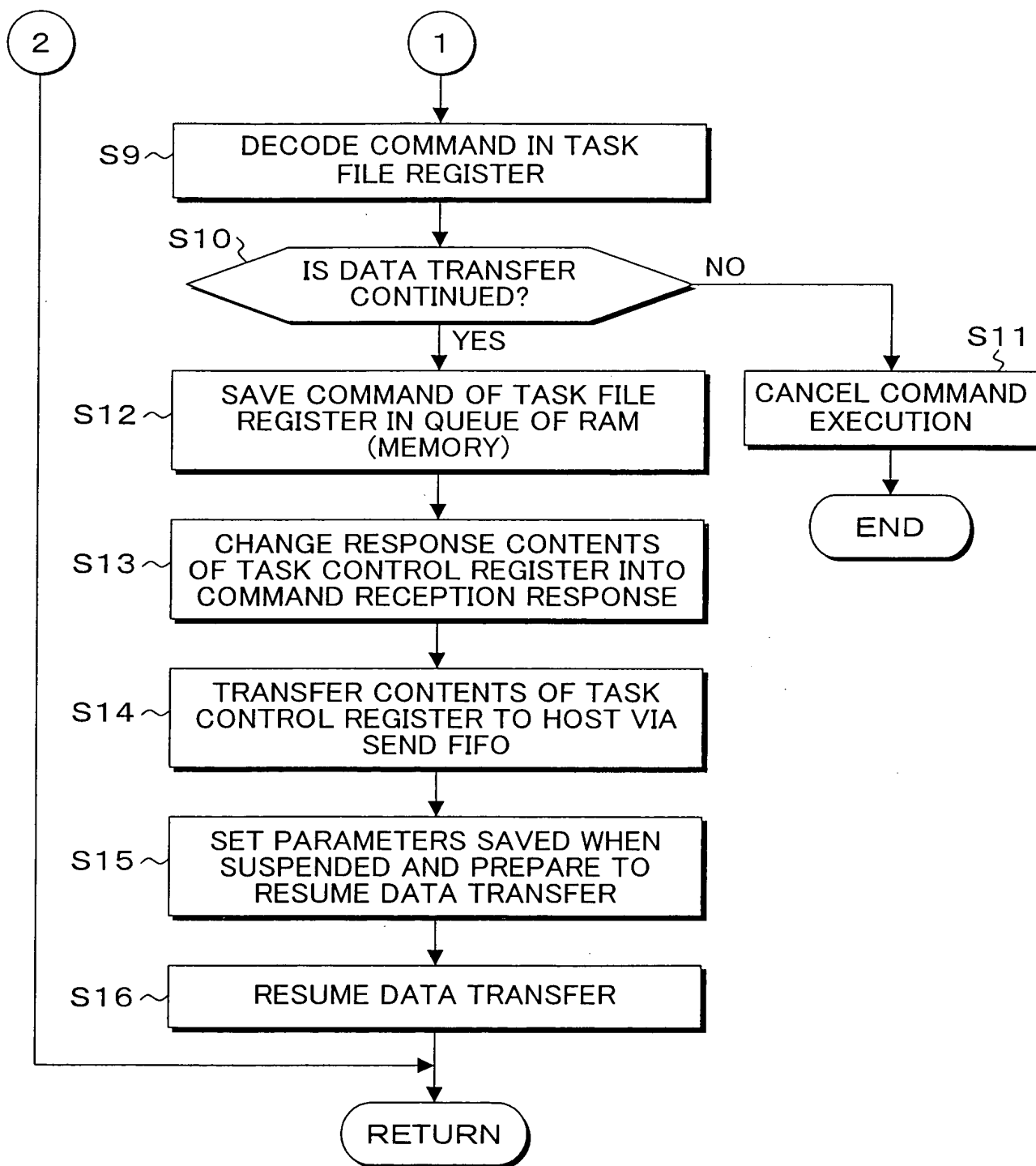
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FIG. 16A



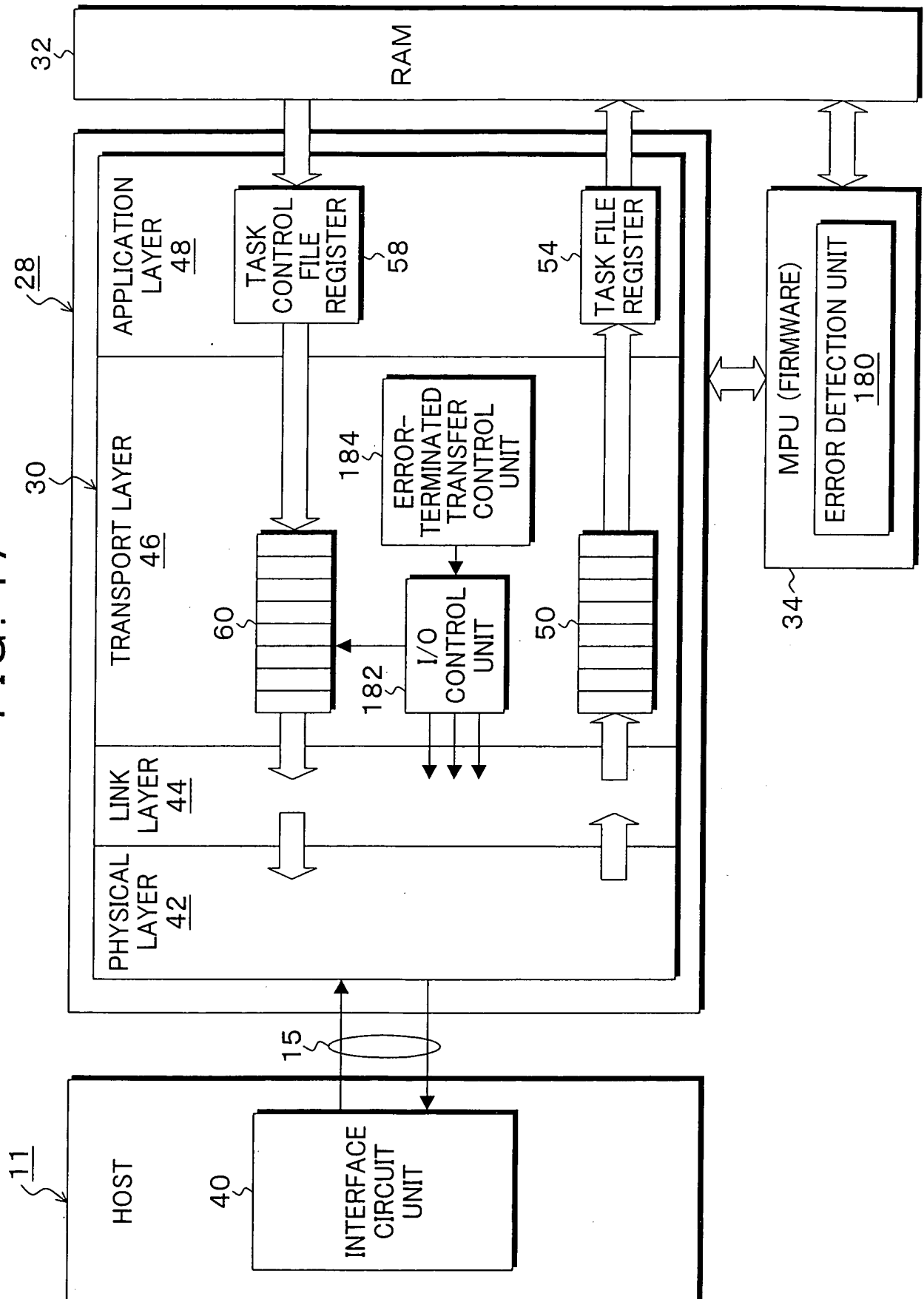
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FIG. 16B



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FIG. 17



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FIG. 18A

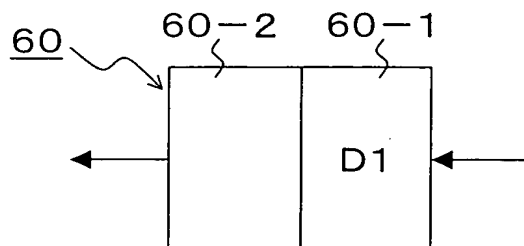


FIG. 18B

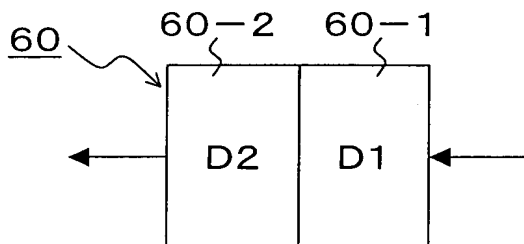


FIG. 18C

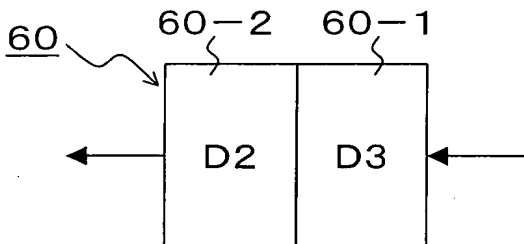
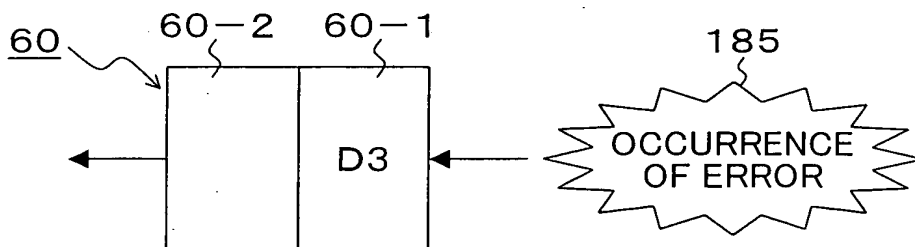


FIG. 18D



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FIG. 19A

INPUT VALID
SIGNAL



FIG. 19B

INPUT HEAD
SIGNAL



FIG. 19C

INPUT TAIL
SIGNAL

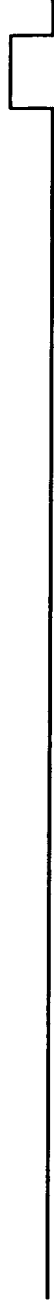


FIG. 19D

INPUT DATA

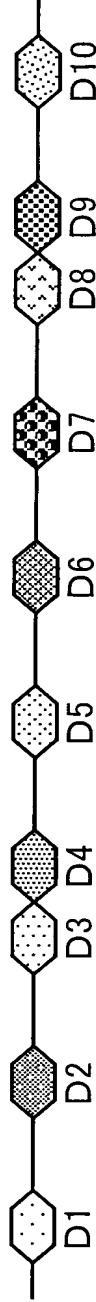


FIG. 19E

OUTPUT VALID
SIGNAL



FIG. 19F

OUTPUT HEAD
SIGNAL



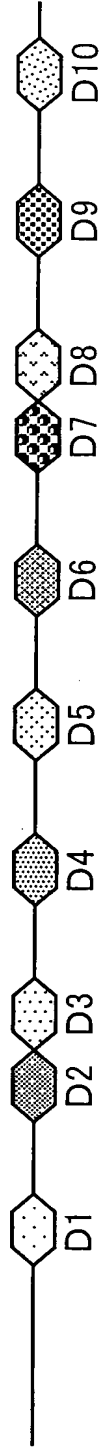
FIG. 19G

OUTPUT TAIL
SIGNAL



FIG. 19H

OUTPUT DATA



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FIG. 20A

INPUT VALID
SIGNAL



FIG. 20B

INPUT HEAD
SIGNAL

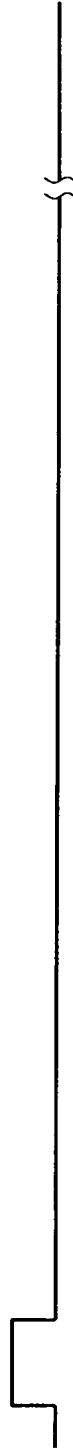


FIG. 20C

INPUT TAIL
SIGNAL



FIG. 20D

INPUT DATA

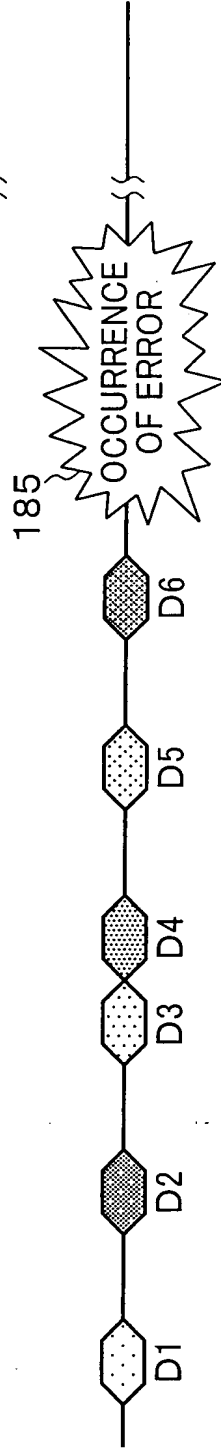


FIG. 20E

OUTPUT VALID
SIGNAL

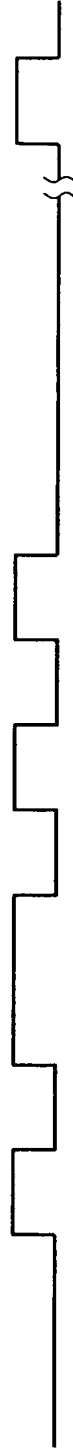


FIG. 20F

OUTPUT HEAD
SIGNAL



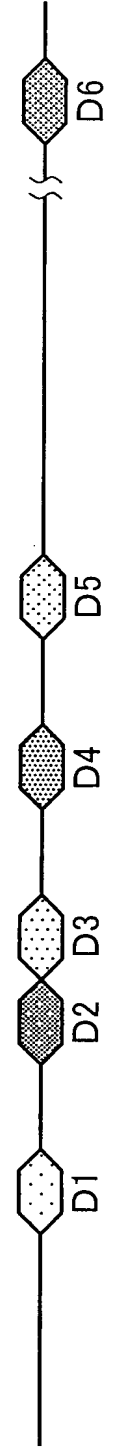
FIG. 20G

OUTPUT TAIL
SIGNAL



FIG. 20H

OUTPUT DATA



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FIG. 21A

INPUT VALID
SIGNAL



FIG. 21B

INPUT HEAD
SIGNAL



FIG. 21C

INPUT TAIL
SIGNAL



FIG. 21D

INPUT DATA

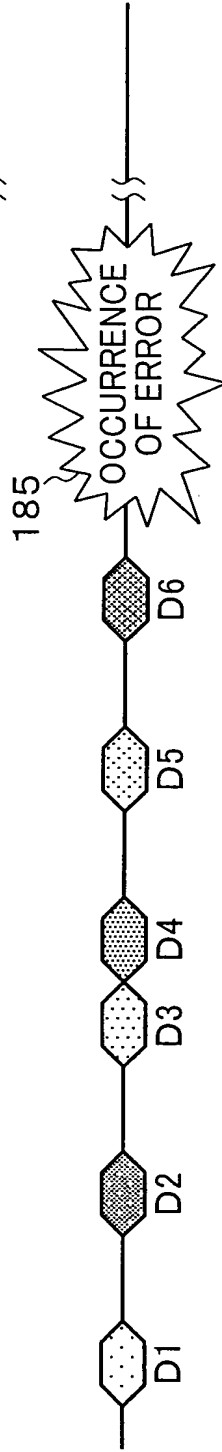


FIG. 21E

OUTPUT VALID
SIGNAL



FIG. 21F

OUTPUT HEAD
SIGNAL



FIG. 21G

OUTPUT TAIL
SIGNAL

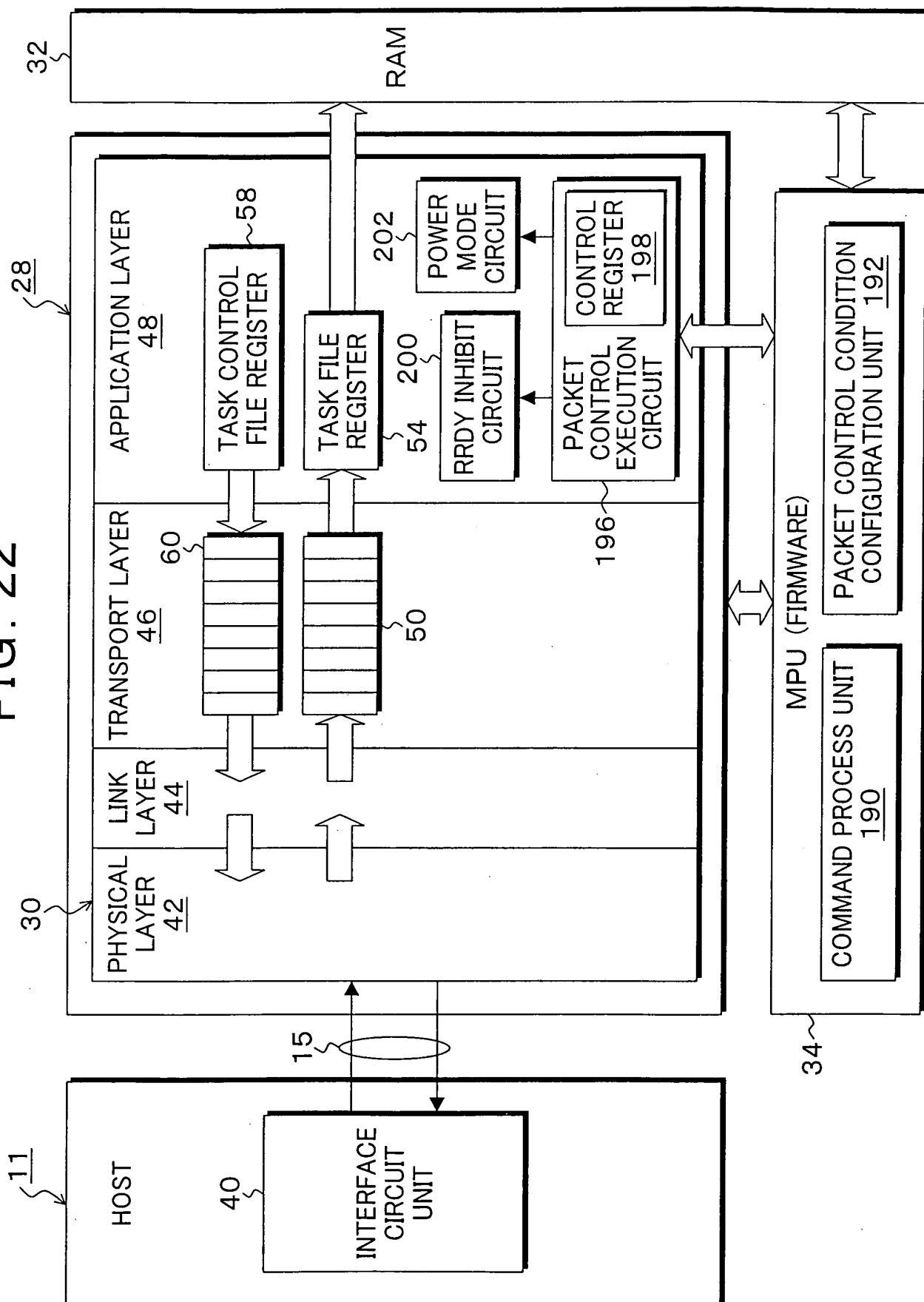


FIG. 21H

OUTPUT DATA



FIG. 22



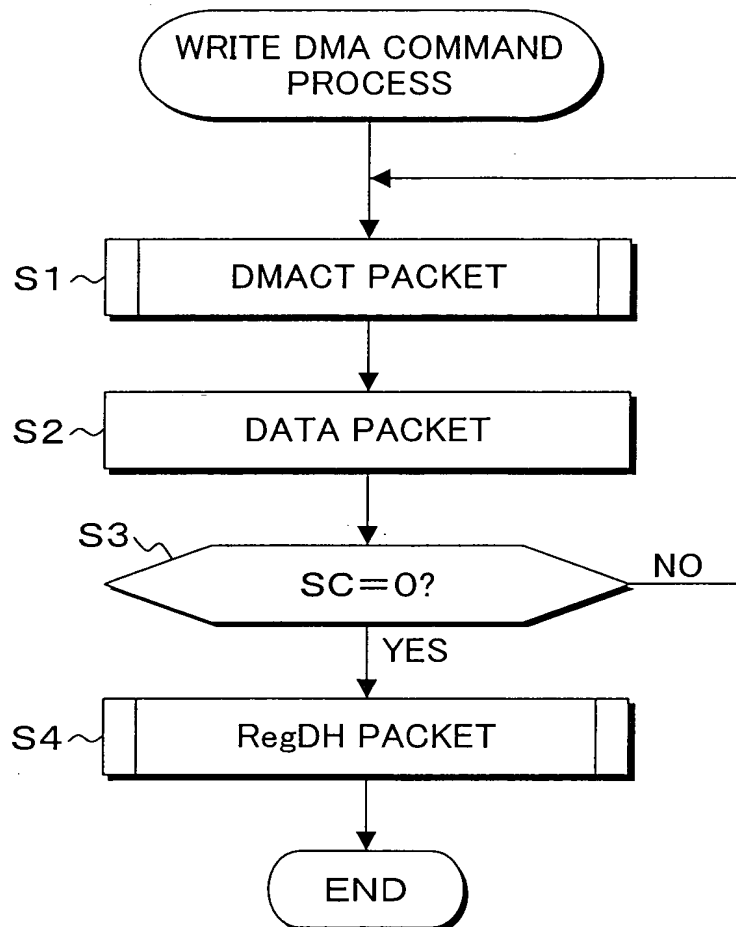
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FIG. 23

		<u>198</u>			
BIT	15	14	13	12 0
FUNCTION	RRDY INHIBITION	RDDY INHIBITION CANCELLATION	POWER MODE	NUMBER OF PACKETS	
	204	206	208	210	

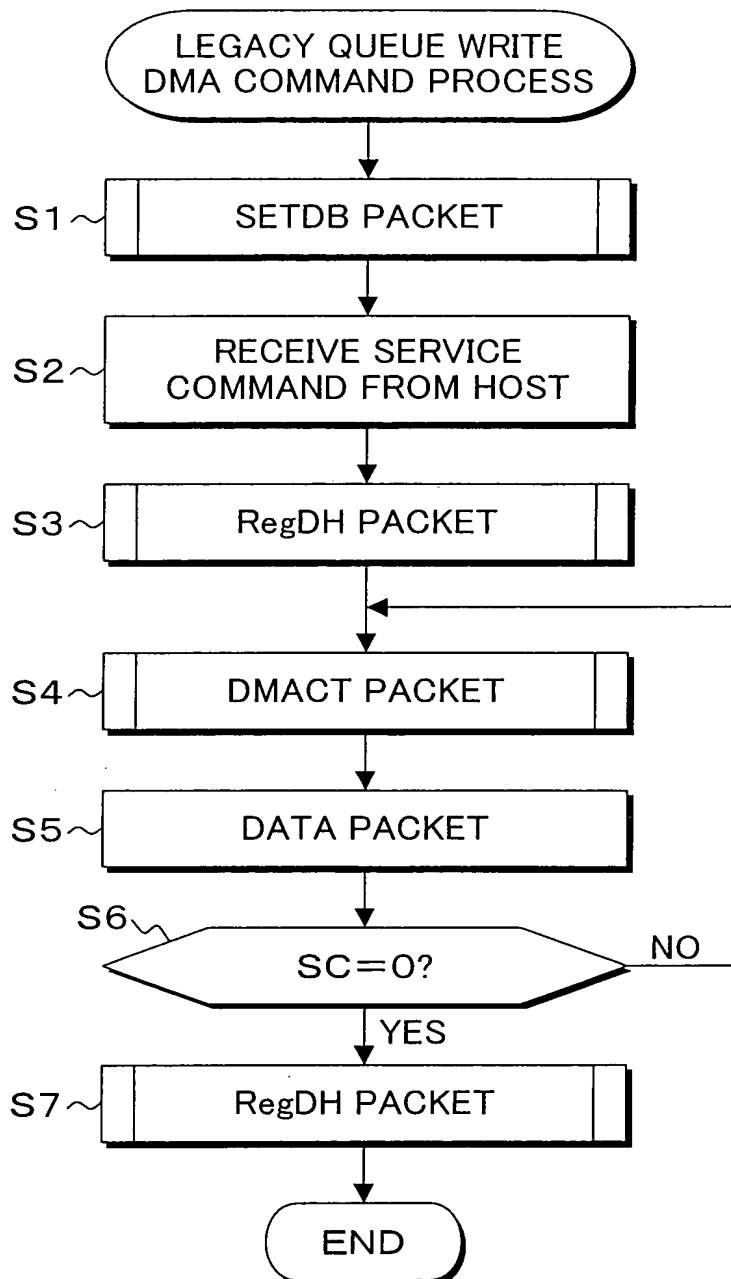
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FIG. 24



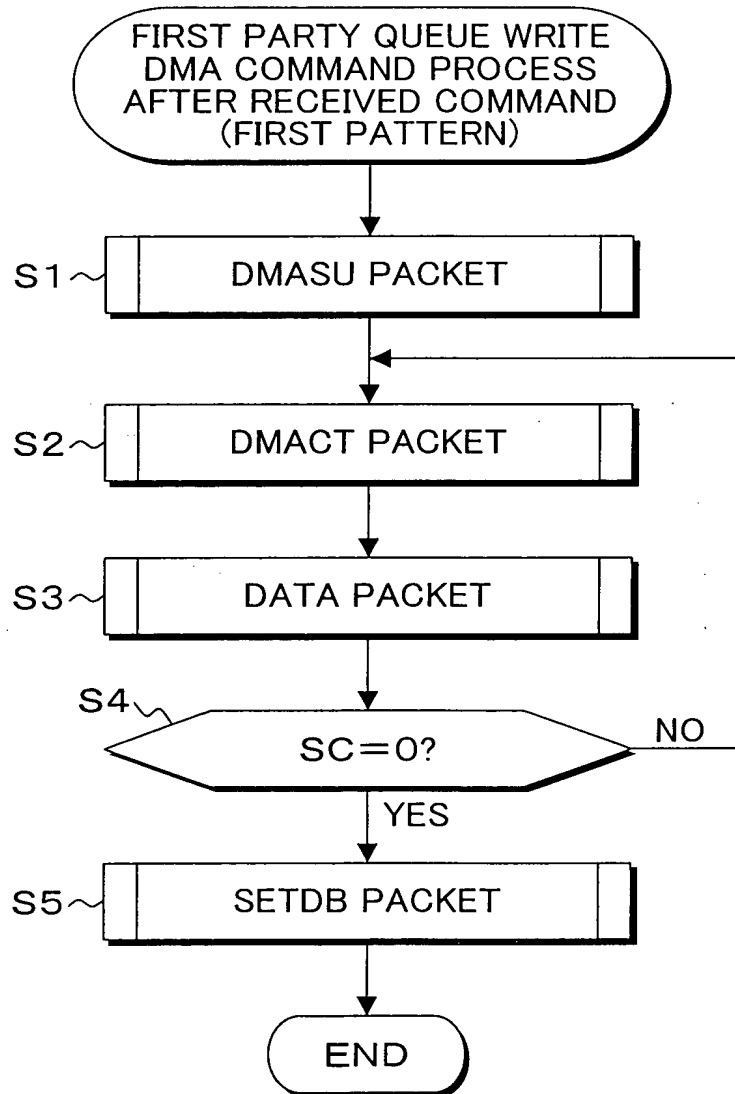
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FIG. 25



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FIG. 26



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FIG. 27

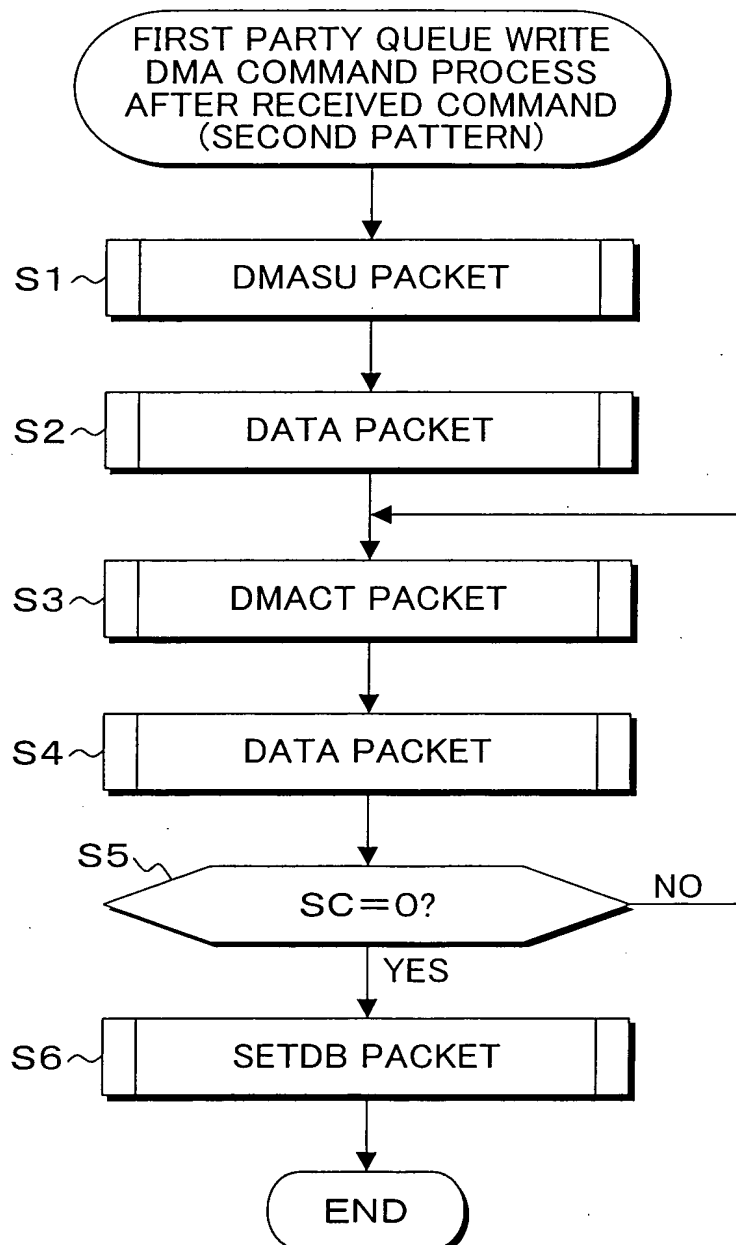
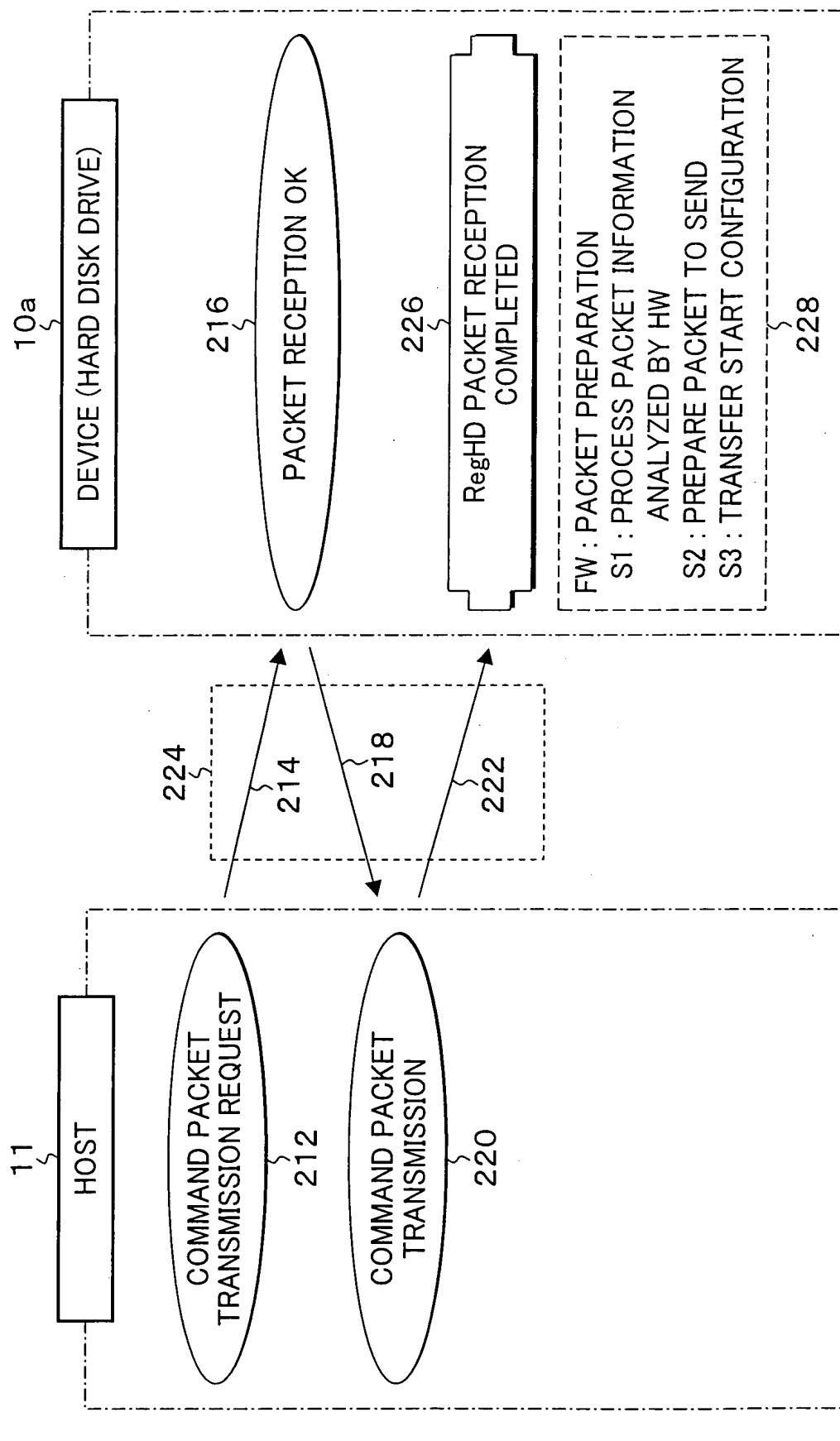
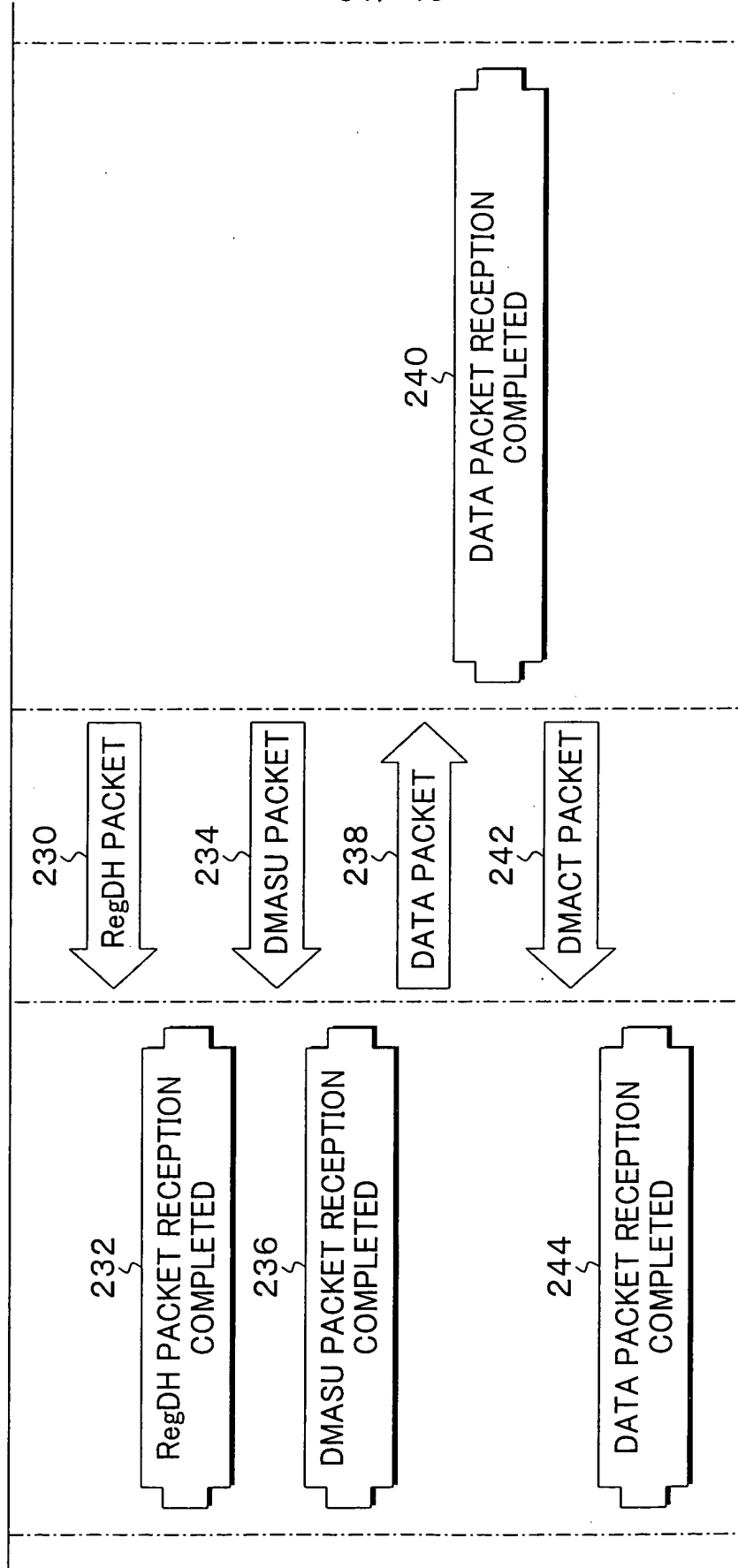


FIG. 28A



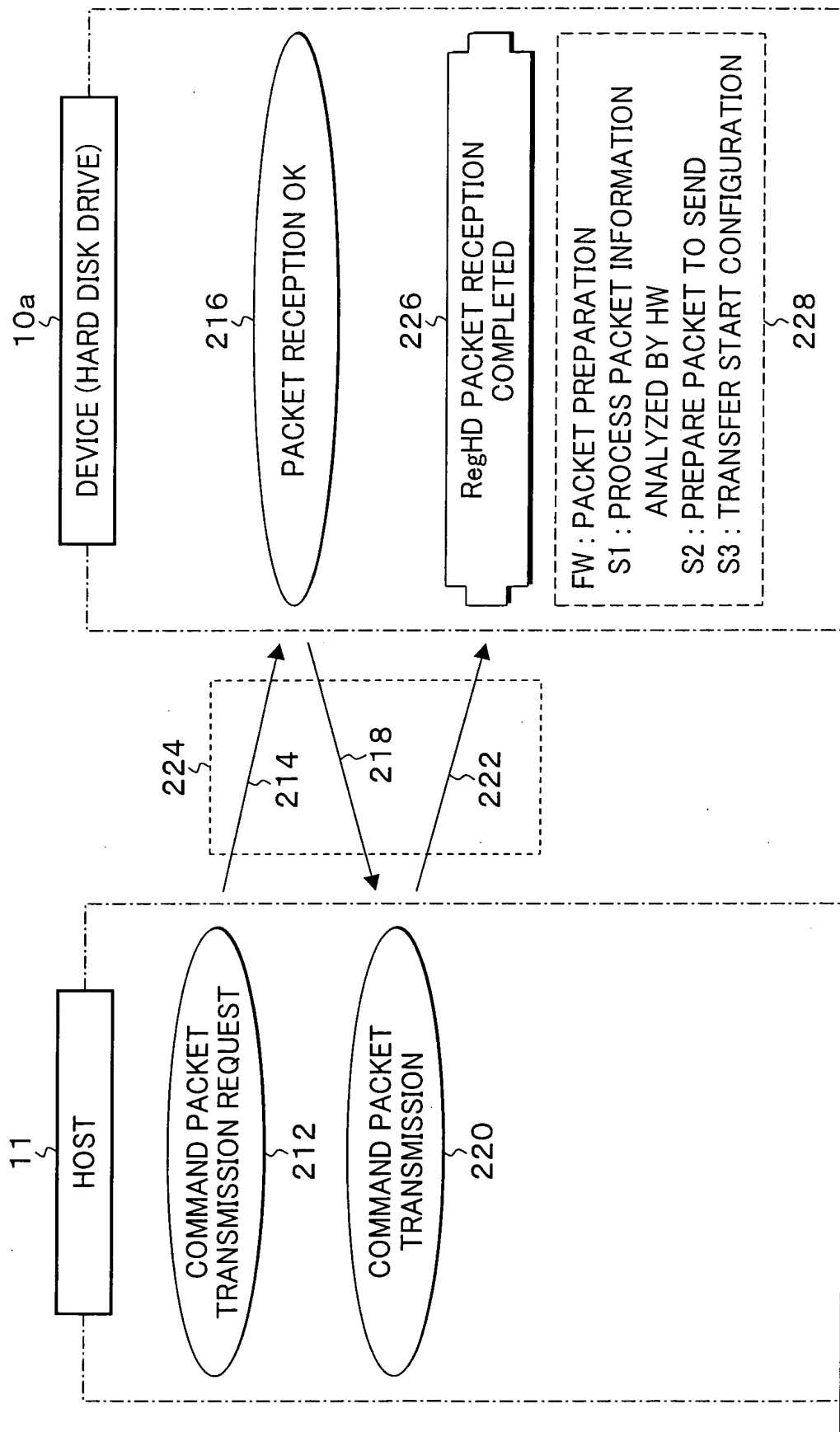
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FIG. 28B



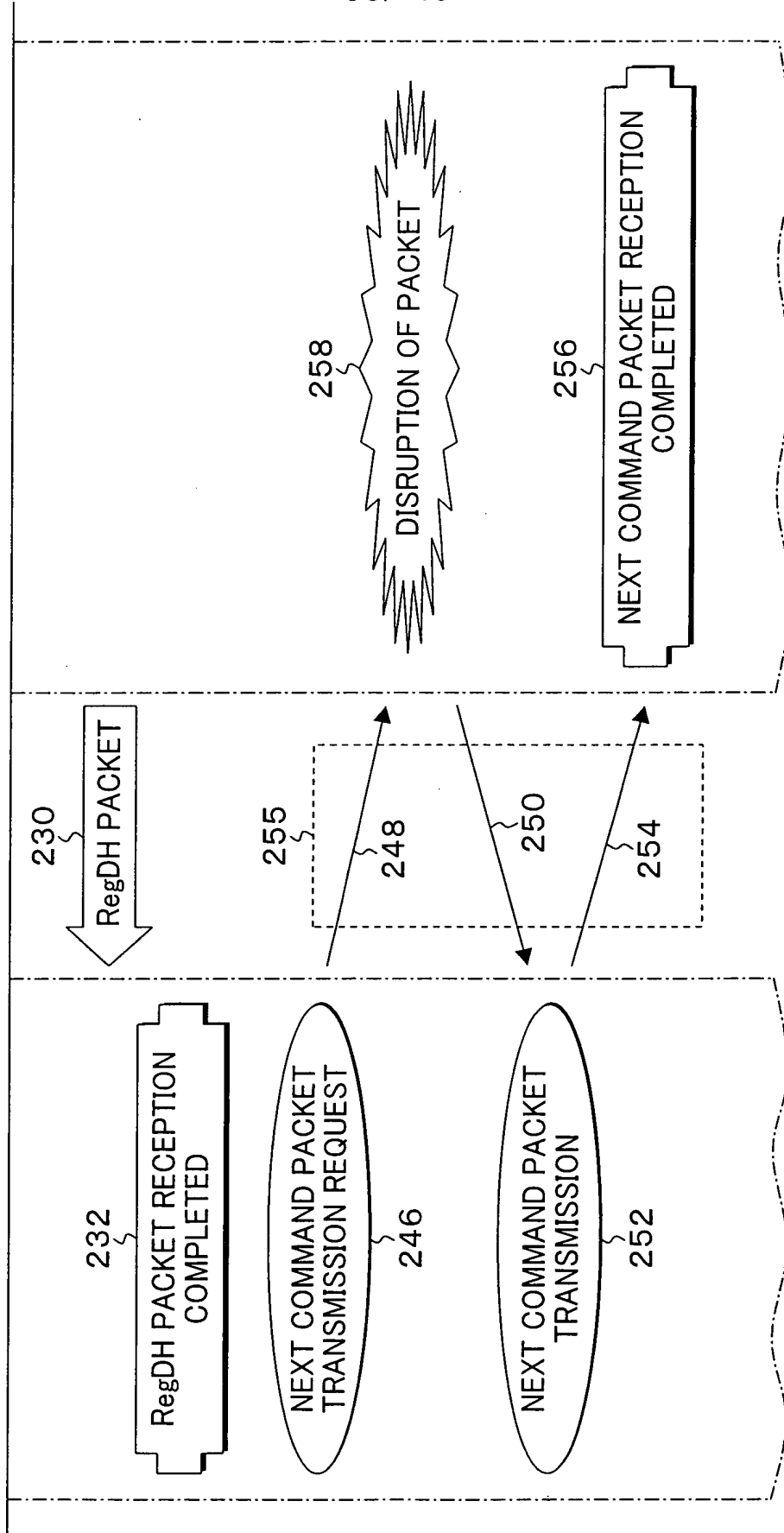
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FIG. 29A



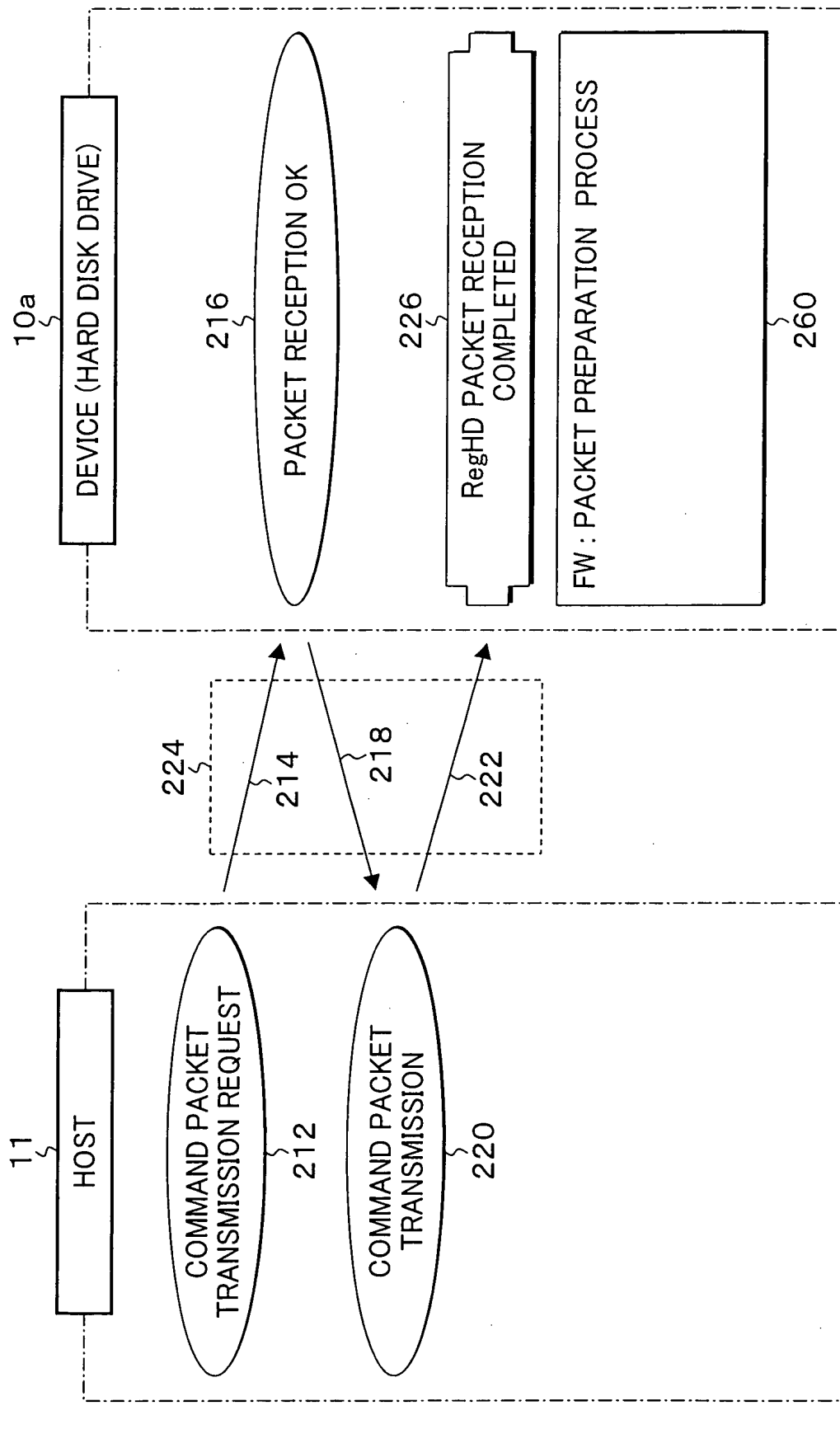
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FIG. 29B



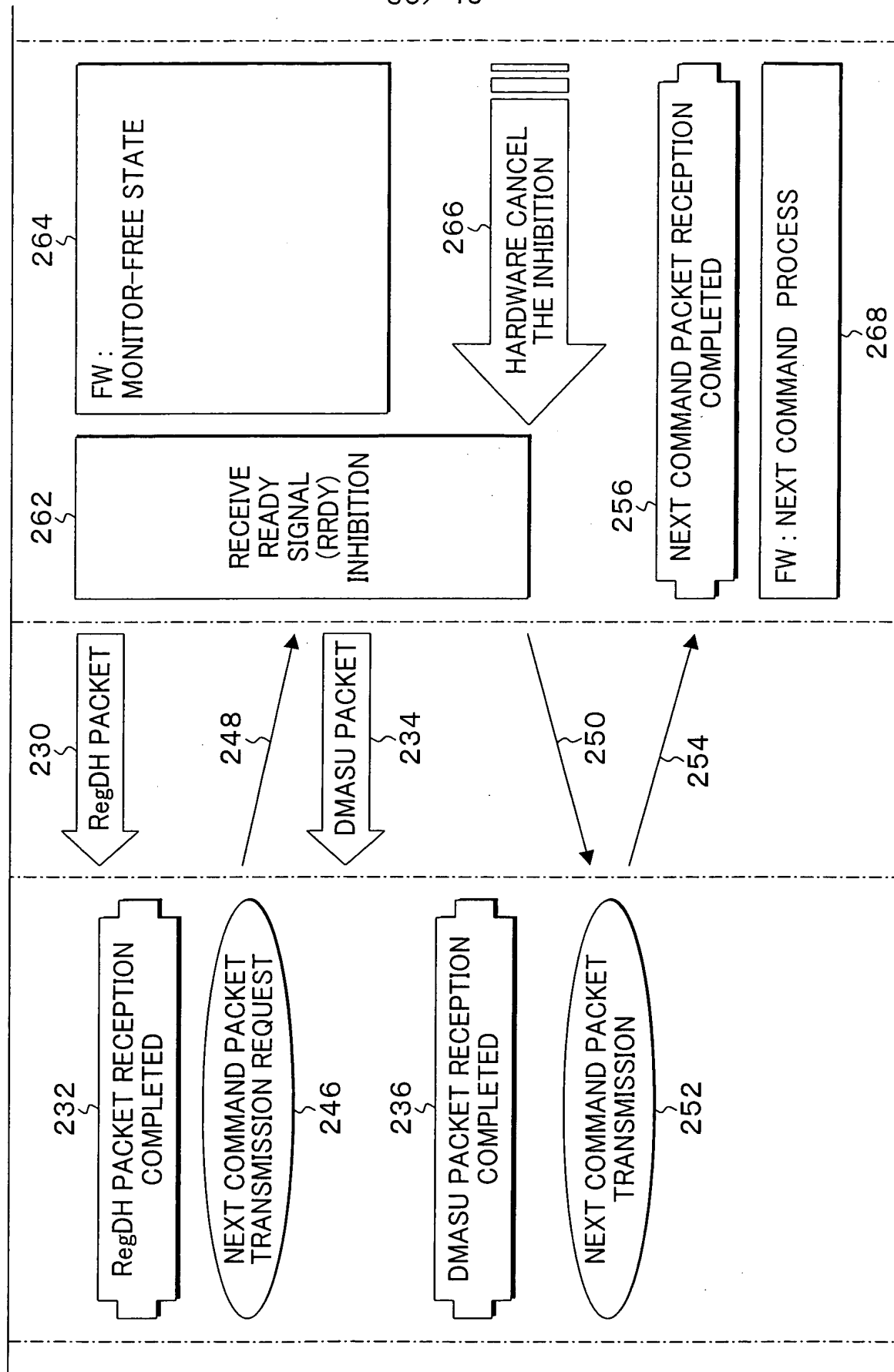
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FIG. 30A



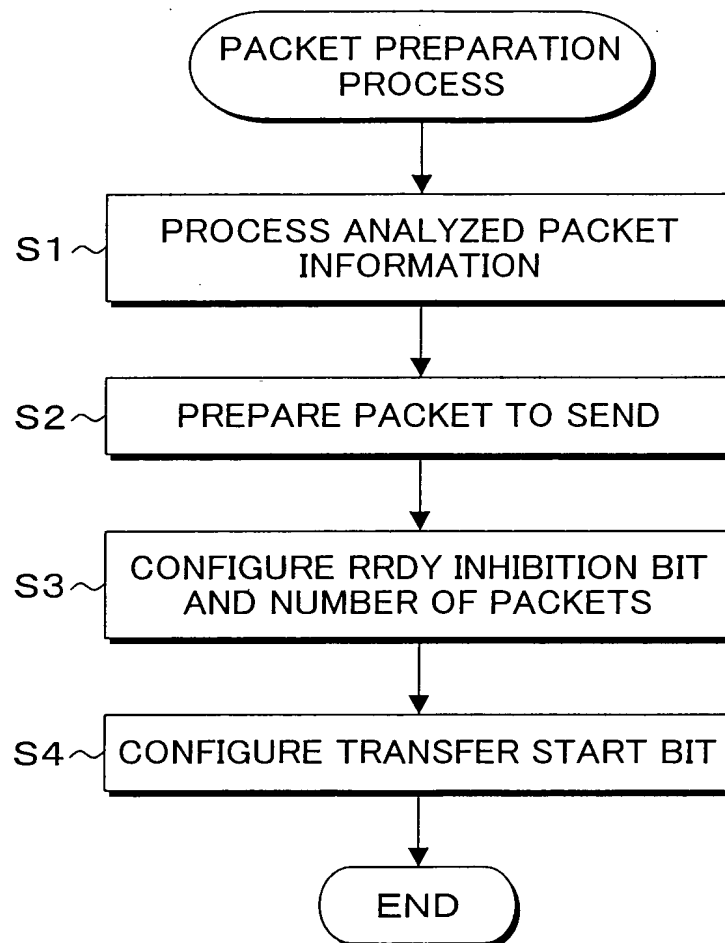
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FIG. 30B



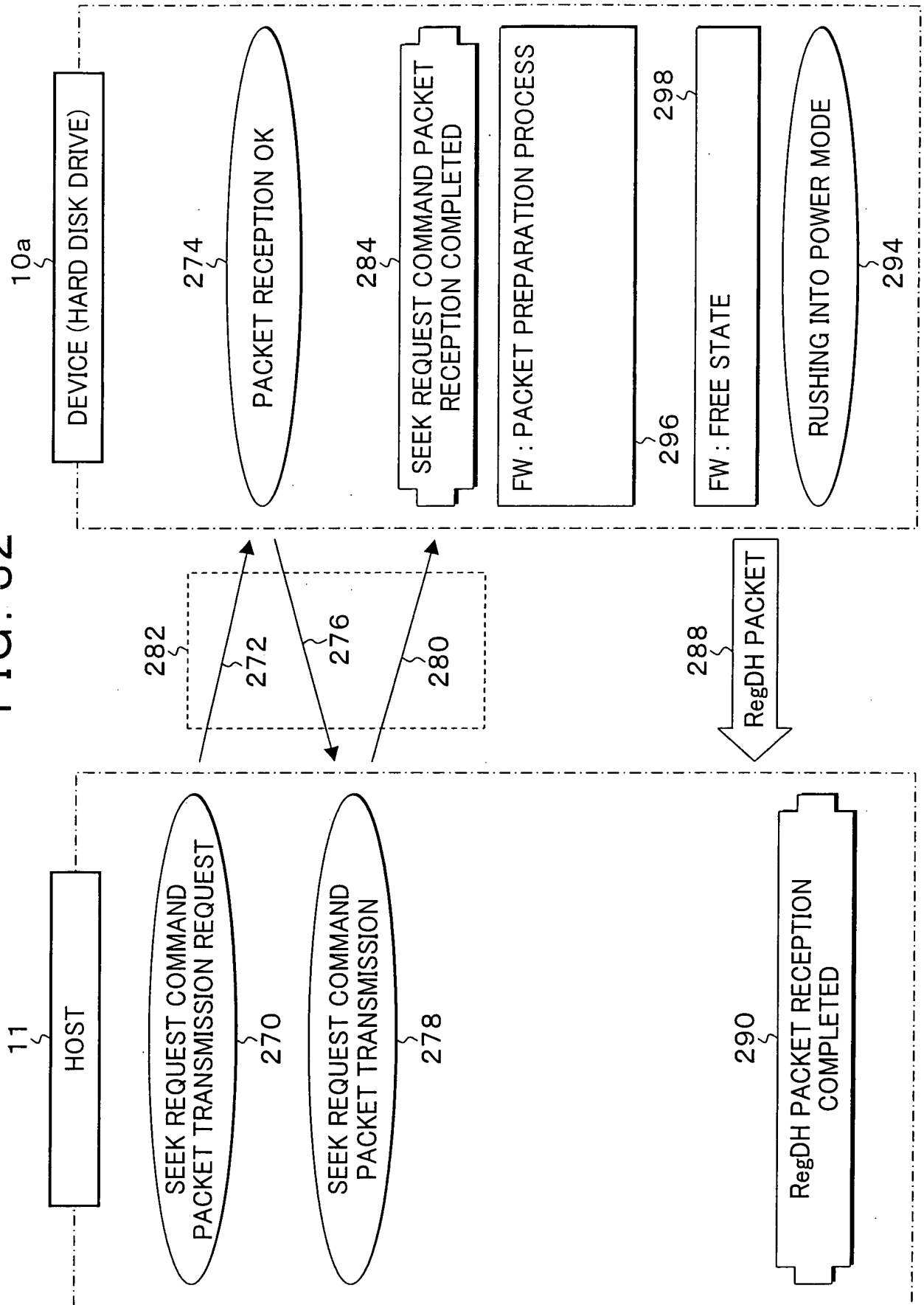
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FIG. 31



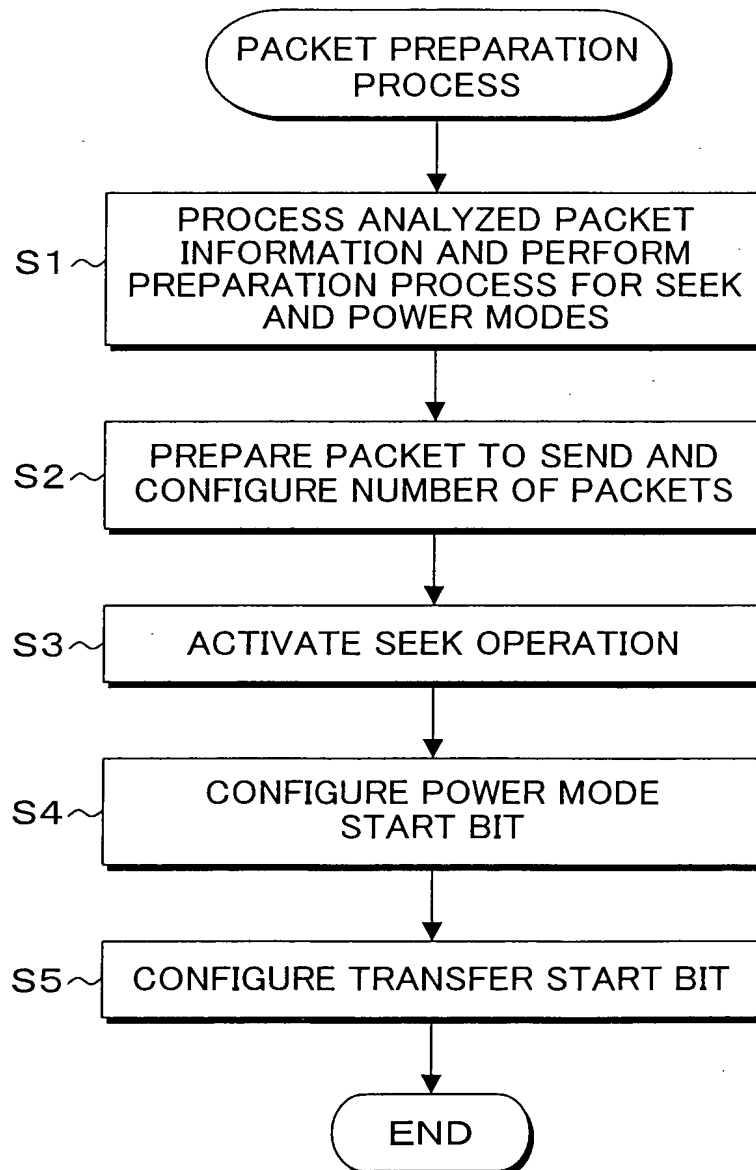
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FIG. 32



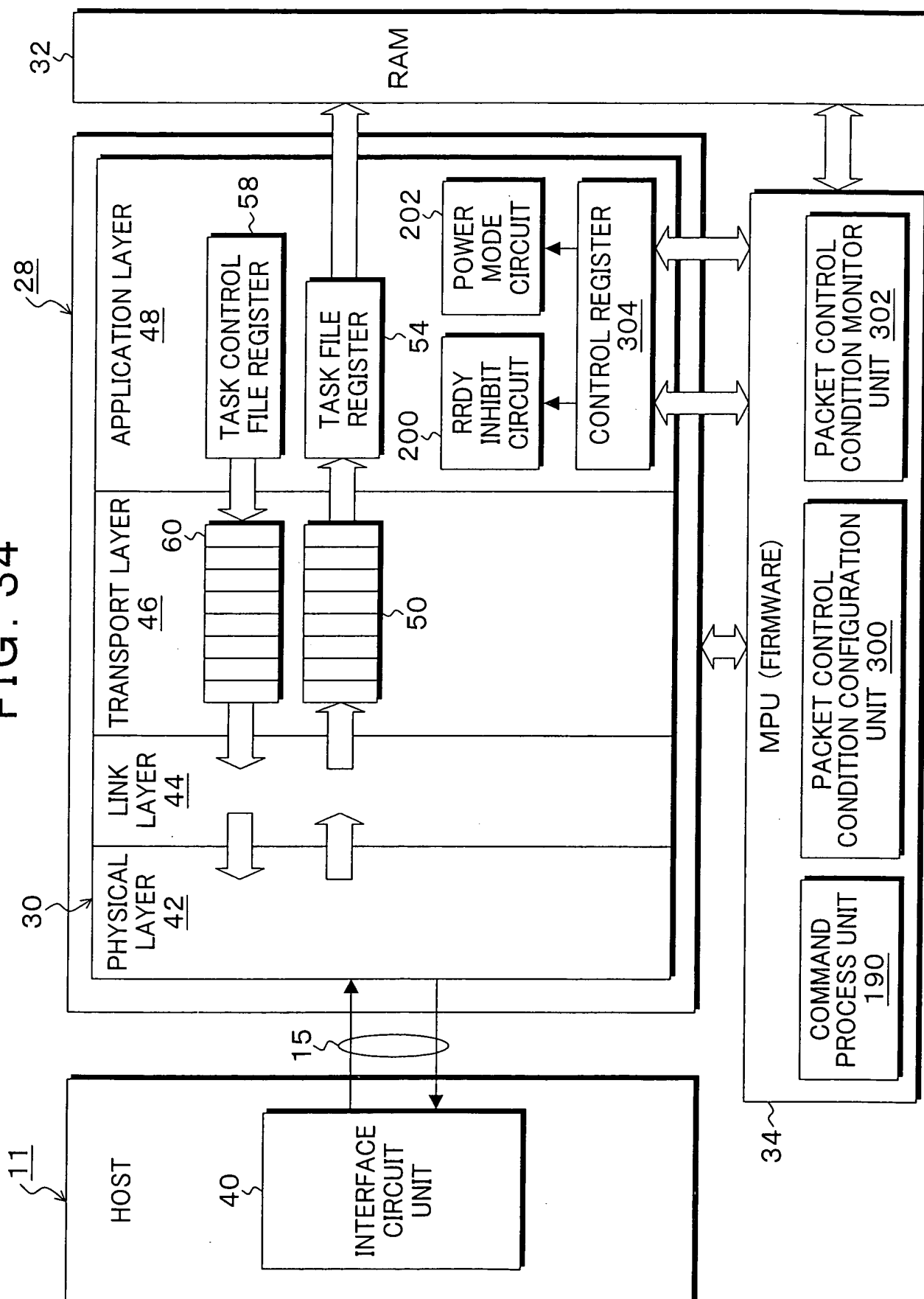
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FIG. 33



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FIG. 34



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FIG. 35

BIT	15	14	13	12	0
FUNCTION	RRDY INHIBITION	RDDY INHIBITION CANCELLATION	POWER MODE		

304

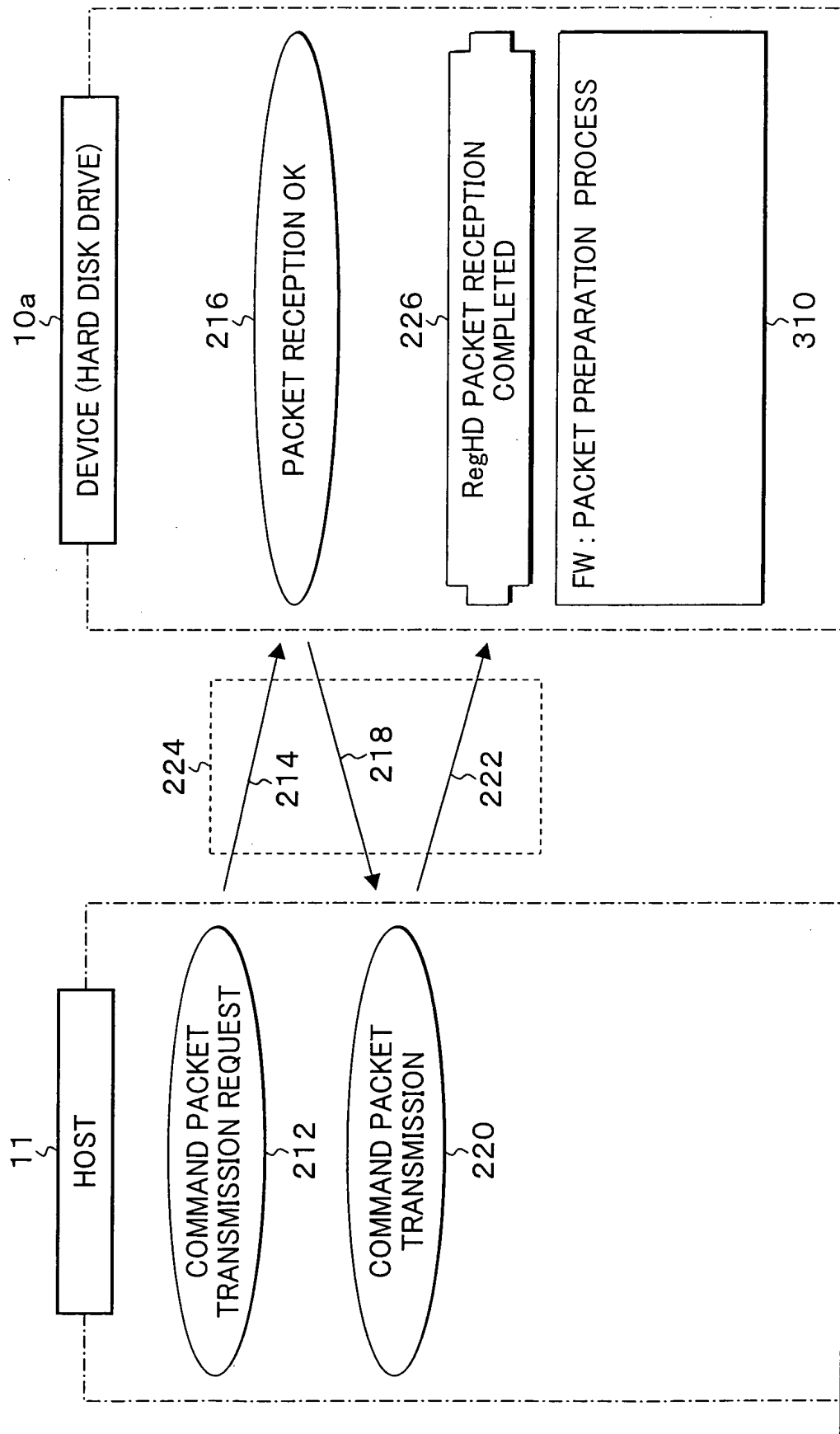
305

306

308

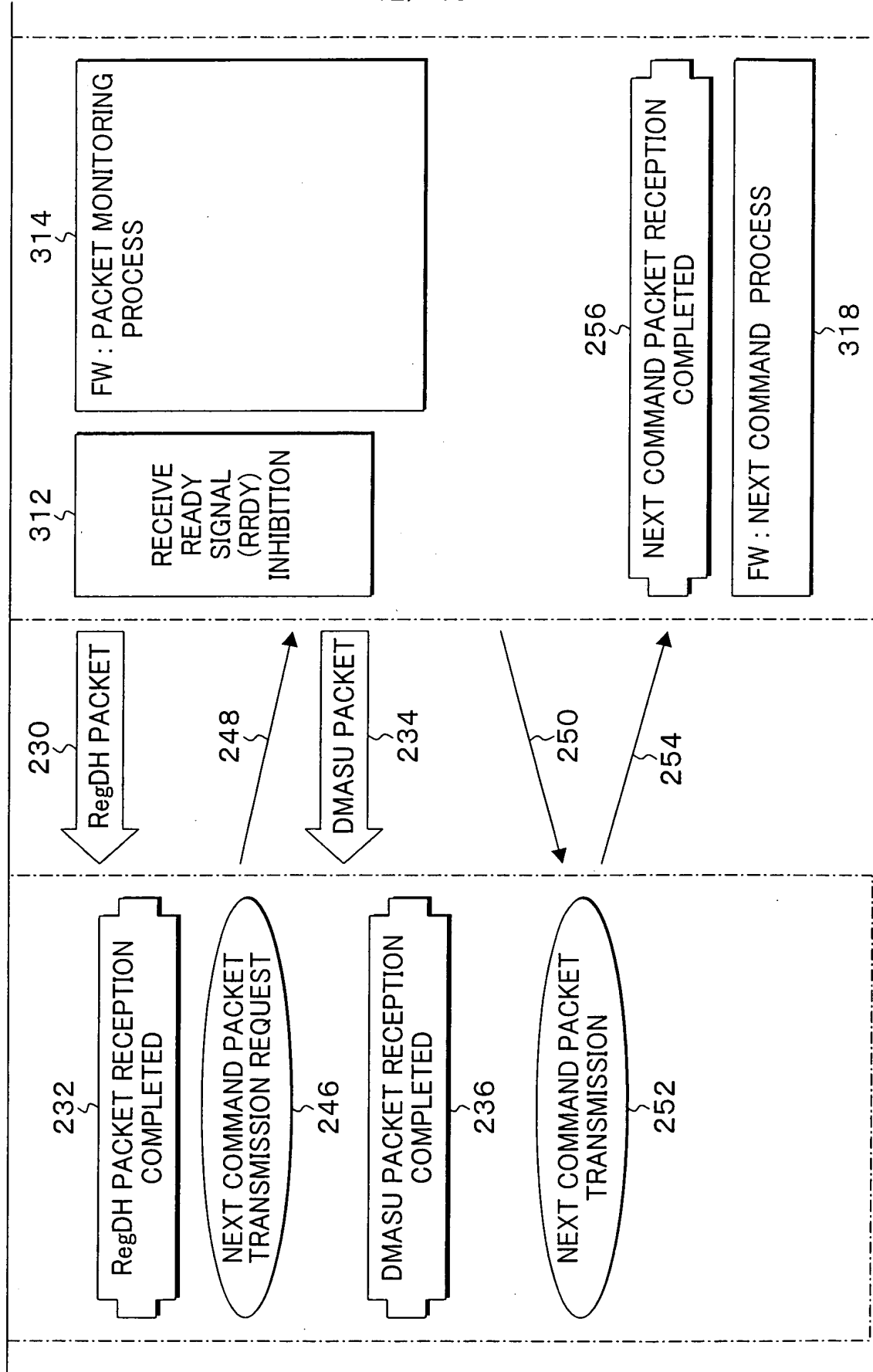
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FIG. 36A



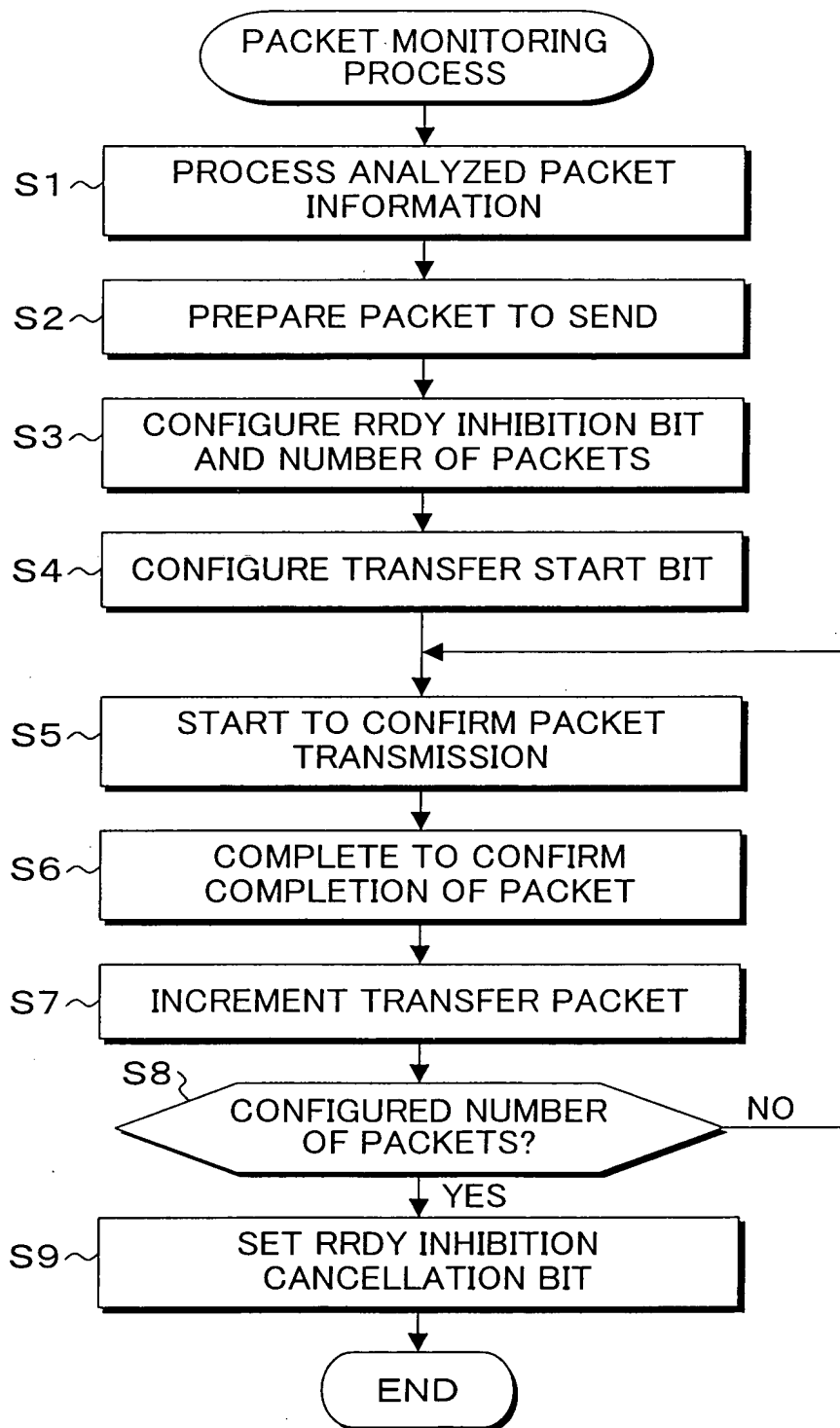
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FIG. 36B



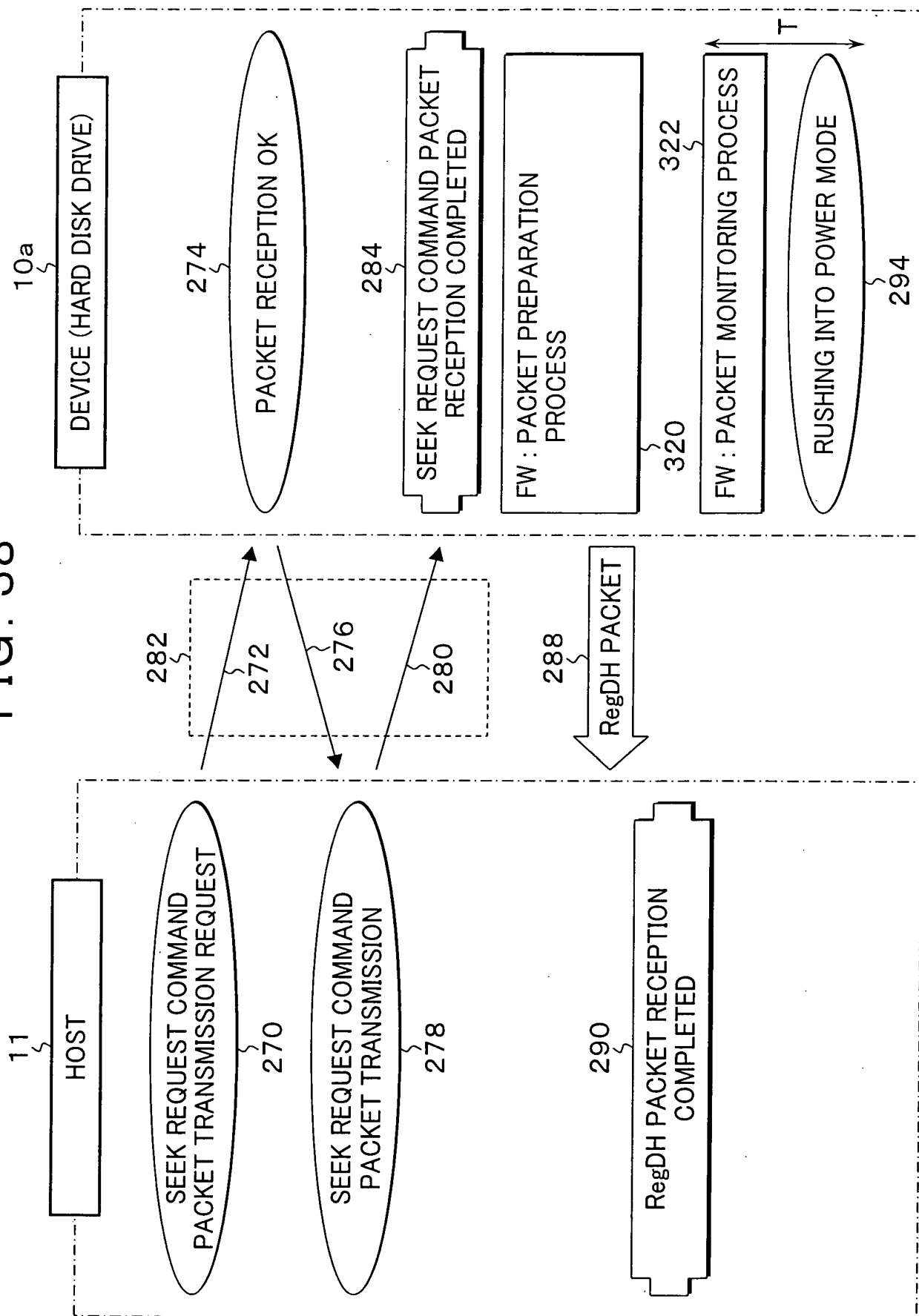
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FIG. 37



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FIG. 38



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FIG. 39

